

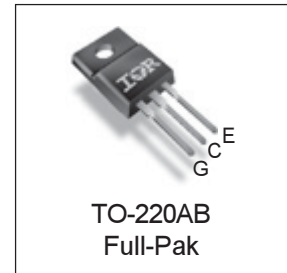
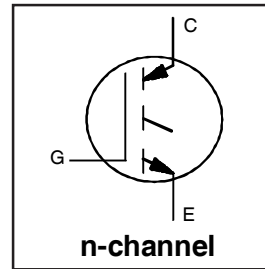
PDP TRENCH IGBT

IRG6IC30UPbF

Features

- Advanced Trench IGBT Technology
- Optimized for Sustain and Energy Recovery circuits in PDP applications
- Low $V_{CE(on)}$ and Energy per Pulse (E_{PULSE}^{TM}) for improved panel efficiency
- High repetitive peak current capability
- Lead Free package

Key Parameters		
$V_{CE\ min}$	600	V
$V_{CE(ON)}\ typ.\ @\ I_C = 25A$	1.50	V
$I_{RP}\ max\ @\ T_C = 25^\circ C\ ①$	250	A
$T_J\ max$	150	°C



G	C	E
Gate	Collector	Emitter

Description

This IGBT is specifically designed for applications in Plasma Display Panels. This device utilizes advanced trench IGBT technology to achieve low $V_{CE(on)}$ and low E_{PULSE}^{TM} rating per silicon area which improve panel efficiency. Additional features are 150°C operating junction temperature and high repetitive peak current capability. These features combine to make this IGBT a highly efficient, robust and reliable device for PDP applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{GE}	Gate-to-Emitter Voltage	±30	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current, $V_{GE} @ 15V$	25	A
$I_C @ T_C = 100^\circ C$	Continuous Collector, $V_{GE} @ 15V$	12	
$I_{RP} @ T_C = 25^\circ C$	Repetitive Peak Current ①	250	
$P_D @ T_C = 25^\circ C$	Power Dissipation	37	W
$P_D @ T_C = 100^\circ C$	Power Dissipation	15	
	Linear Derating Factor	0.30	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-40 to + 150	°C
	Soldering Temperature for 10 seconds	300	
	Mounting Torque, 6-32 or M3 Screw	10lb·in (1.1N·m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ②	—	3.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient ②	—	65	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{CES}	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V _{GE} = 0V, I _{CE} = 1.0mA
V _{(BR)ECS}	Emitter-to-Collector Breakdown Voltage ^③	15	—	—	V	V _{GE} = 0V, I _{CE} = 1.0A
ΔBV _{CES} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.49	—	V/°C	Reference to 25°C, I _{CE} = 1mA
V _{CE(on)}	Static Collector-to-Emitter Voltage	—	1.29	—	V	V _{GE} = 15V, I _{CE} = 12A ^③
		—	1.50	1.92		V _{GE} = 15V, I _{CE} = 25A ^③
		—	1.73	—		V _{GE} = 15V, I _{CE} = 40A ^③
		—	2.16	—		V _{GE} = 15V, I _{CE} = 70A ^③
		—	2.88	—		V _{GE} = 15V, I _{CE} = 120A ^③
		—	1.51	—		V _{GE} = 15V, I _{CE} = 25A, T _J = 150°C ^③
V _{GE(th)}	Gate Threshold Voltage	2.6	—	5.0	V	V _{CE} = V _{GE} , I _{CE} = 500μA
ΔV _{GE(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	-8.9	—	mV/°C	
I _{CES}	Collector-to-Emitter Leakage Current	—	2.0	20	μA	V _{CE} = 600V, V _{GE} = 0V
		—	10	—		V _{CE} = 600V, V _{GE} = 0V, T _J = 100°C
		—	40	100		V _{CE} = 600V, V _{GE} = 0V, T _J = 125°C
		—	150	—		V _{CE} = 600V, V _{GE} = 0V, T _J = 150°C
I _{GES}	Gate-to-Emitter Forward Leakage	—	—	100	nA	V _{GE} = 30V
	Gate-to-Emitter Reverse Leakage	—	—	-100	nA	V _{GE} = -30V
g _{fe}	Forward Transconductance	—	32	—	S	V _{CE} = 25V, I _{CE} = 25A
Q _g	Total Gate Charge	—	79	—	nC	V _{CE} = 400V, I _C = 25A, V _{GE} = 15V ^③
Q _{gc}	Gate-to-Collector Charge	—	30	—	nC	
t _{d(on)}	Turn-On delay time	—	20	—	ns	I _C = 25A, V _{CC} = 400V R _G = 10Ω, L=200μH T _J = 25°C
t _r	Rise time	—	16	—		
t _{d(off)}	Turn-Off delay time	—	160	—		
t _f	Fall time	—	120	—		
t _{d(on)}	Turn-On delay time	—	18	—	ns	I _C = 25A, V _{CC} = 400V R _G = 10Ω, L=200μH T _J = 150°C
t _r	Rise time	—	17	—		
t _{d(off)}	Turn-Off delay time	—	190	—		
t _f	Fall time	—	240	—		
t _{st}	Shoot Through Blocking Time	100	—	—	ns	V _{CC} = 240V, V _{GE} = 15V, R _G = 5.1Ω
E _{PULSE}	Energy per Pulse	—	1020	—	μJ	L = 220nH, C = 0.40μF, V _{GE} = 15V V _{CC} = 240V, R _G = 5.1Ω, T _J = 25°C
		—	1150	—		L = 220nH, C = 0.40μF, V _{GE} = 15V V _{CC} = 240V, R _G = 5.1Ω, T _J = 100°C
ESD	Human Body Model	Class 2 (Per JEDEC standard JESD22-A114)				
	Machine Model	Class B (Per EIA/JEDEC standard EIA/JESD22-A115)				
C _{ies}	Input Capacitance	—	2390	—	pF	V _{GE} = 0V
C _{oes}	Output Capacitance	—	85	—		V _{CE} = 30V
C _{res}	Reverse Transfer Capacitance	—	58	—		f = 1.0MHz, See Fig.13
L _C	Internal Collector Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.)
L _E	Internal Emitter Inductance	—	7.5	—		from package and center of die contact

Notes:

- ① Half sine wave with duty cycle ≤ 0.02, ton=1.0μsec.
- ② R_θ is measured at T_J of approximately 90°C.
- ③ Pulse width ≤ 400μs; duty cycle ≤ 2%.

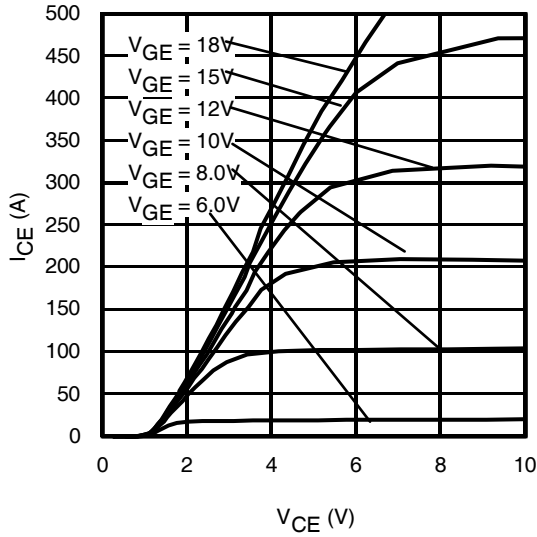


Fig 1. Typical Output Characteristics @ 25°C

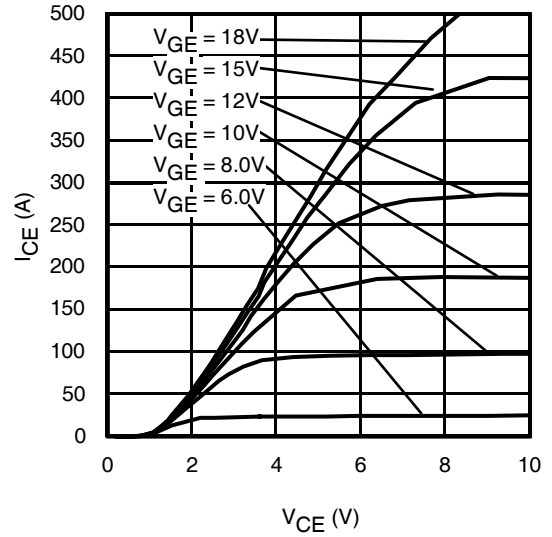


Fig 2. Typical Output Characteristics @ 75°C

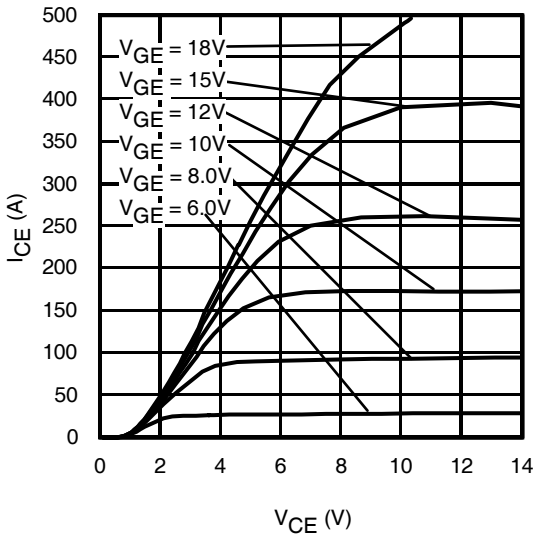


Fig 3. Typical Output Characteristics @ 125°C

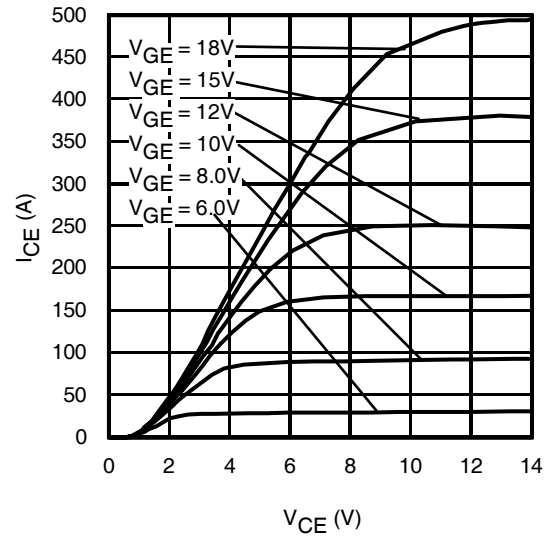


Fig 4. Typical Output Characteristics @ 150°C

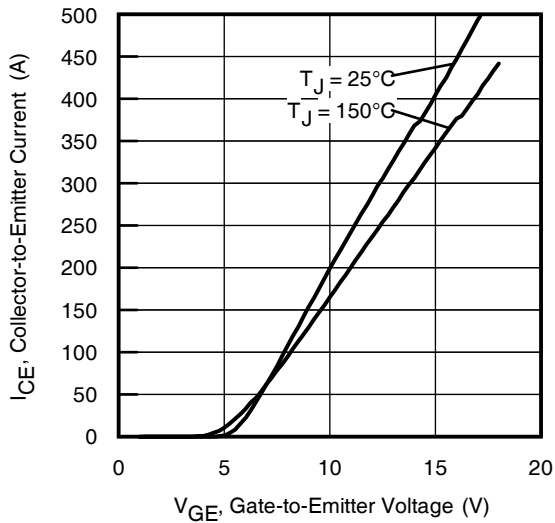


Fig 5. Typical Transfer Characteristics

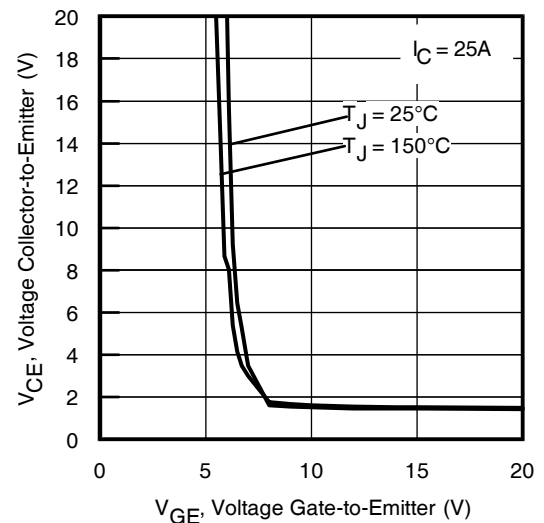


Fig 6. $V_{CE(ON)}$ vs. Gate Voltage

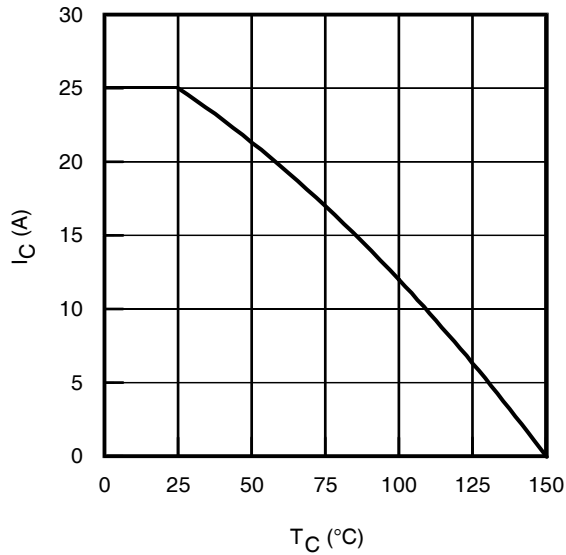


Fig 7. Maximum Collector Current vs. Case Temperature

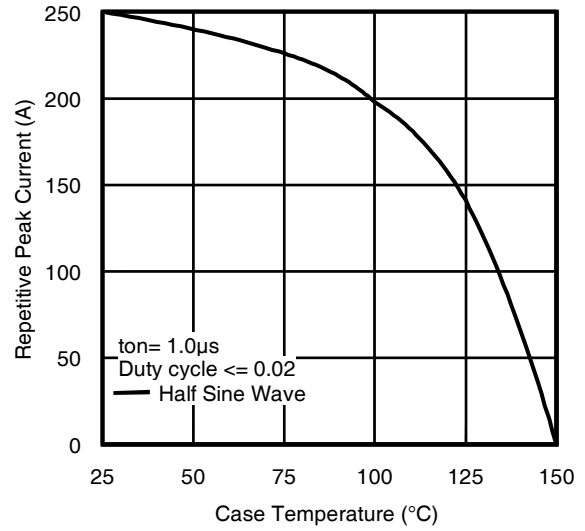


Fig 8. Typical Repetitive Peak Current vs. Case Temperature

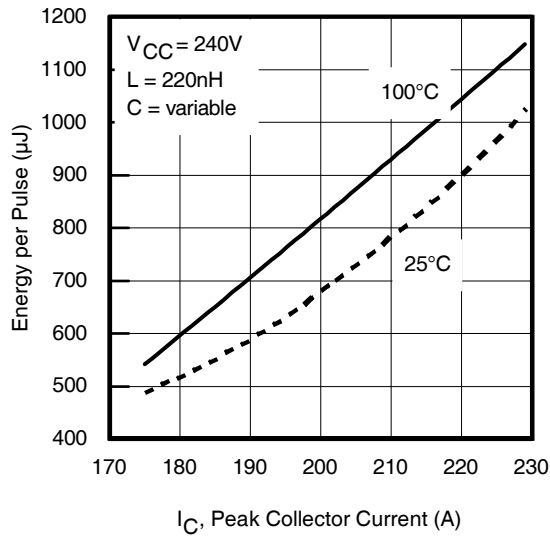


Fig 9. Typical E_{PULSE} vs. Collector Current

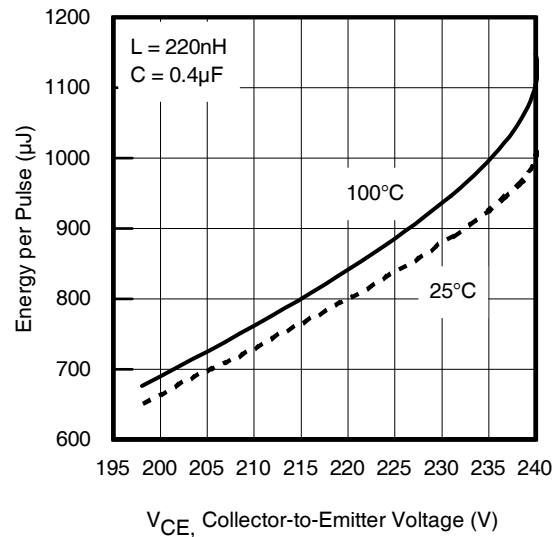


Fig 10. Typical E_{PULSE} vs. Collector-to-Emitter Voltage

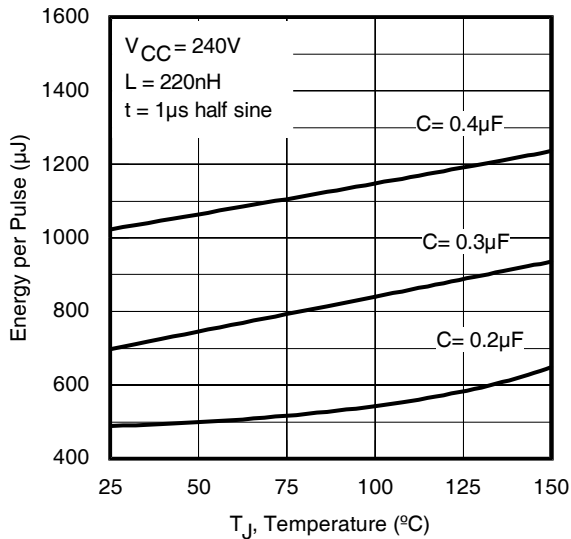


Fig 11. E_{PULSE} vs. Temperature

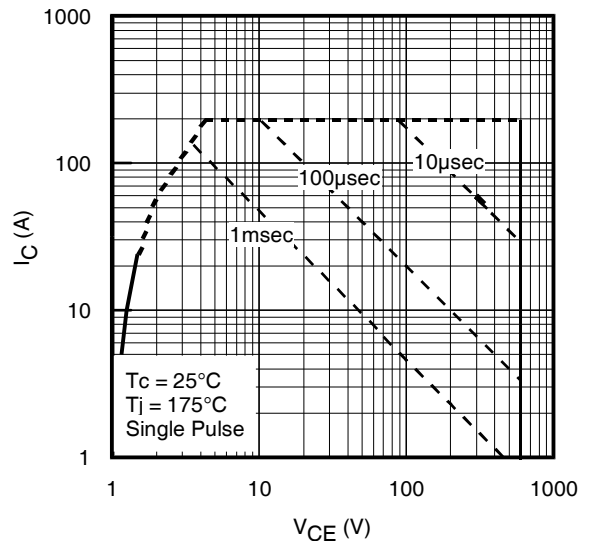


Fig 12. Forward Bias Safe Operating Area

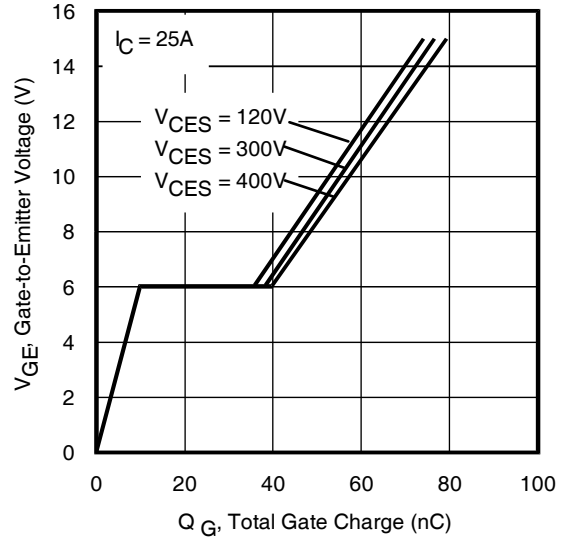
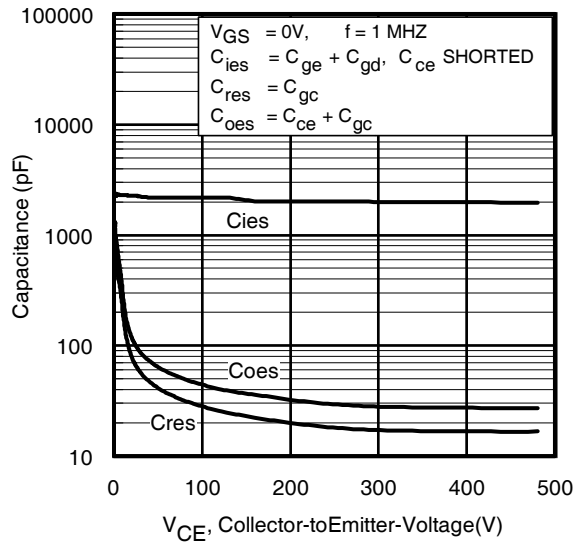


Fig 13. Typical Capacitance vs. Collector-to-Emitter Voltage

Fig 14. Typical Gate Charge vs. Gate-to-Emitter Voltage

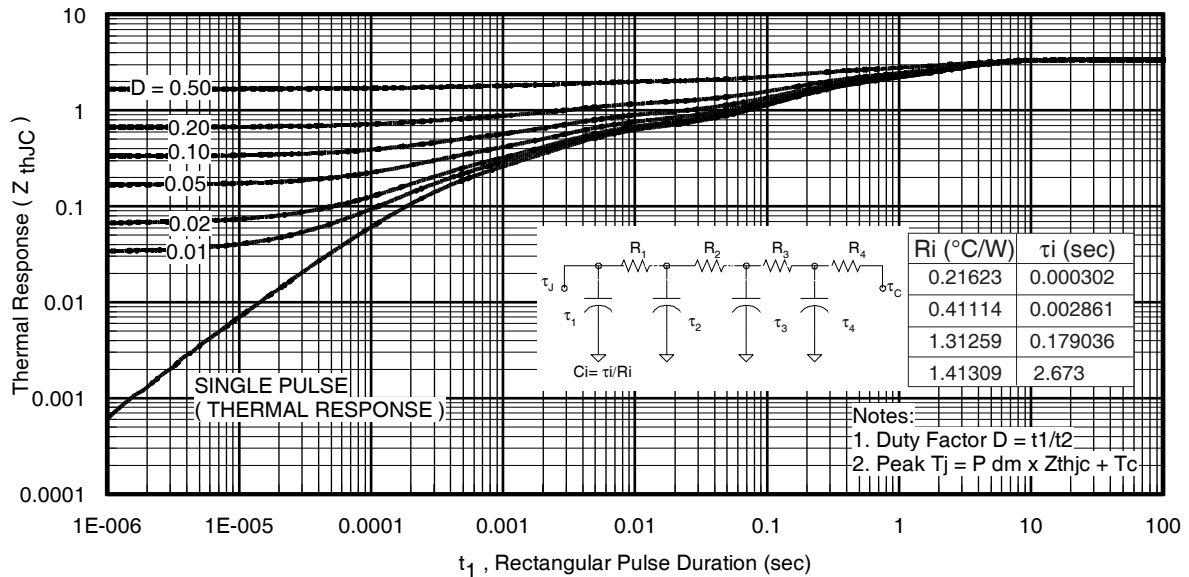


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

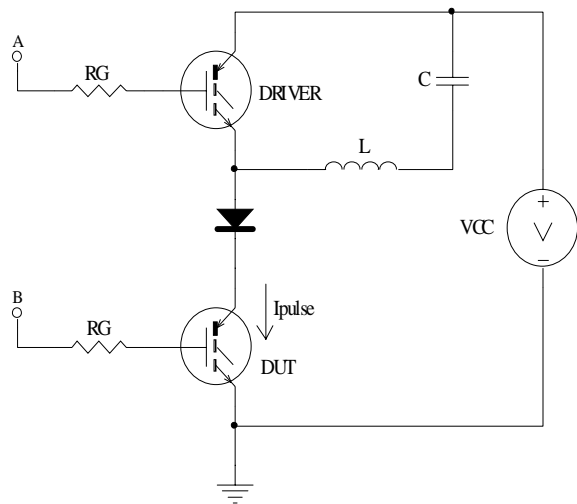


Fig 16a. t_{st} and E_{PULSE} Test Circuit

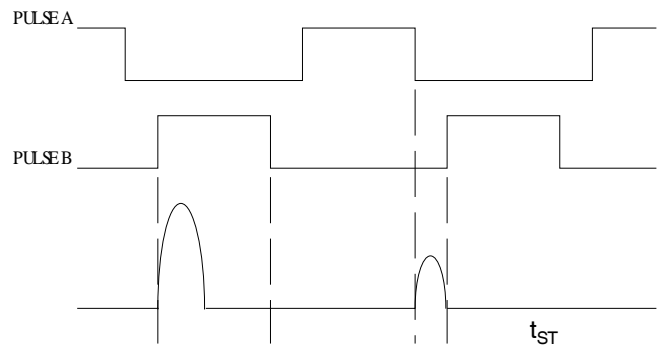


Fig 16b. t_{st} Test Waveforms

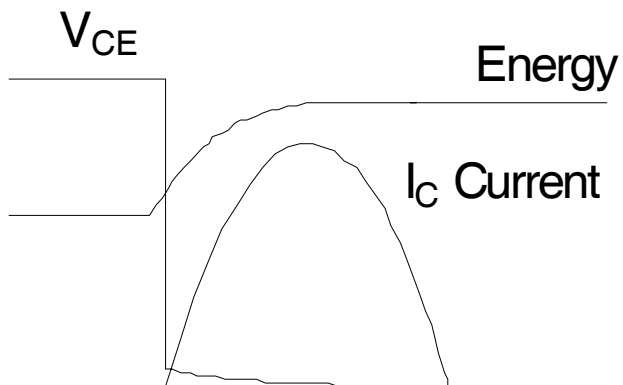


Fig 16c. E_{PULSE} Test Waveforms

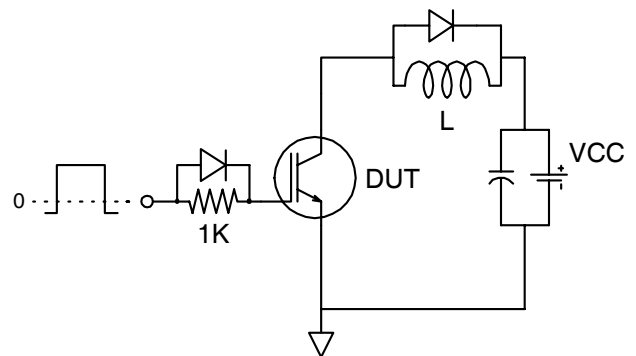
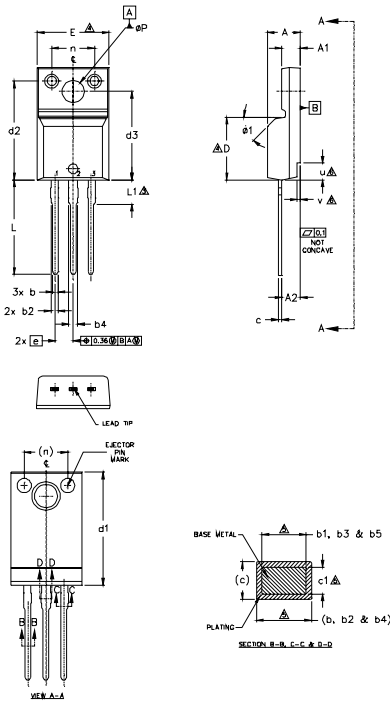


Fig 17 - Gate Charge Circuit (turn-off)

TO-220AB Full-Pak Package Outline

Dimensions are shown in millimeters (inches)

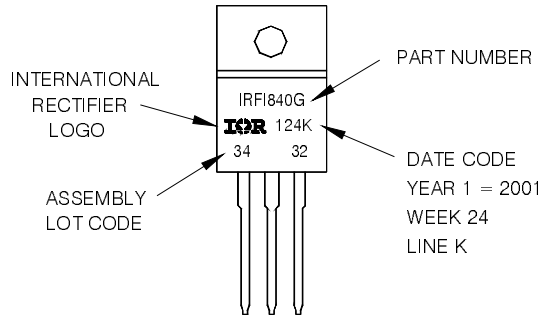


SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.57	4.83	.180	.190	NOTES: 1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994. 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]. 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1. 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY. 5.0 DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY. 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v. 7.0 CONTROLLING DIMENSION : INCHES.
A1	2.57	2.83	.101	.111	
A2	2.51	2.93	.099	.115	
b	0.61	0.94	.024	.037	
b1	0.61	0.89	.024	.035	
b2	0.76	1.27	.030	.050	
b3	0.76	1.22	.030	.048	
b4	1.02	1.52	.040	.060	
b5	1.02	1.47	.040	.058	
c	0.33	0.63	.013	.025	
c1	0.33	0.58	.013	.023	
D	8.66	9.80	.341	.386	
d1	15.80	16.13	.622	.635	
d2	13.97	14.22	.550	.560	
d3	12.30	12.93	.484	.509	
e	9.63	10.75	.379	.423	
e	2.54	BSC	.100	BSC	
L	13.20	13.72	.520	.540	LEAD ASSIGNMENTS HEXFEET 1.- GATE 2.- DRAIN 3.- SOURCE IRG6IC30UPbF 1.- GATE 2.- COLLECTOR 3.- EMITTER
L1	3.37	3.67	.122	.145	
n	6.05	6.60	.238	.260	
phi P	3.05	3.45	.120	.136	6 6
u	2.40	2.50	.094	.098	
v	0.40	0.50	.016	.020	
phi 1	-	45°	-	45°	

TO-220AB Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G
 WITH ASSEMBLY
 LOT CODE 3432
 ASSEMBLED ON WW 24, 2001
 IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position indicates "Lead-Free"



TO-220AB Full-Pak package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

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