TUA 6041-2

Low Power 3-Band Digital TV / Portable Tuner IC with Digital Alignment

LIGHTNING

Communication Solutions

Never stop thinking

Edition 2006-12-19

Published by
Infineon Technologies AG
81726 München, Germany

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Revision History:	**2006-12-19**	**Data Sheet, Revision 3.1**
Previous Version:	2006-09-12	Preliminary Specification, Revision 3.0

Page	Subjects (major changes since last revision)
9 - **11**, **28**, **30** - **41**	L-Band application added. Operating range and AC/DC Characteristics extended for L-Band.
31 - **41**	Table Footnote added with description for impedance measurement.

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Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

horst.klein@infineon.com

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1 Product Info

General Description

The **TUA 6041-2** integrates the mixer-oscillator, AGC amplifier, digitally programmable phase lock loop (PLL) and a digital alignment feature so that traditional air coils can be replaced by SMD coils. This makes the **TUA 6041-2** an ideal product for applications where size and low power consumption are required design key factors. Typical applications include TV's, VCR's, Set Top Boxes (STB) and also a range of portable products.

Features

General

- Suitable for PAL, NTSC, SECAM, DVB, DMB, DAB, ISDB-T and ATSC
- High band covers frequency range for L-Band up to 1.5 GHz
- Supply voltage range from 3 to 5.5 V
- Combined small - wide AGC detection
- AGC + AGC buffer output
- Low phase noise
- Full ESD protection
- Qualified according to JEDEC for consumer applications

Mixer/Oscillator

- Three band tuner
- Unbalanced highohmic LOW band input
- Balanced lowohmic MID band input
- Balanced lowohmic HIGH band input
- Two pin oscillators for LOW/MID band
- Four pin oscillator for HIGH band

IF-Amplifier

- 4 IF pins to connect a 2 pole bandpass
- Symmetrical SAW driver
- Fully balanced IF AGC amplifier

PLL

- I^2C / three wire combi bus
- 4 independent I^2C addresses
- High voltage VCO tuning output
- Two PMOS ports
- One voltage referred port
- Internal LOW/MID/HIGH band switch
- Xtal oscillator, range from 4 to 16 MHz
- Xtal buffer output with programmable level and output divider
- Clock generator for DC/DC converter with programmable high and low time

Digital alignment

- Three DACs for digital alignment, control range up to 5 volt

Power management

- Bus controlled stand by mode

Application

- The IC is suitable for PAL, NTSC, SECAM, DVB-C, DVB-T, DVB-H, DMB-T, DAB, ISDB-T, ATSC and L-Band tuners.

Ordering Information

Type	Ordering Code	Package
TUA 6041-2	SP000250163	PG-VQFN-48

2 Product Description

The **TUA 6041-2** integrates the mixer-oscillator, variable AGC output amplifier, digitally programmable phase lock loop (PLL) not requiring an external high voltage buffer and a digital alignment feature. Furthermore, the **TUA 6041-2** integrates a buffered RF AGC, programmable clock signals for an external DC-DC up converter along with open drain DAC outputs used for automatic digital alignment.

The integrated mixer oscillator function comprises of three balanced mixers. The first mixer has an unbalanced high impedance input while the other two have balance low impedance inputs. The tuner also has firstly, 2-pin asymmetric oscillators for both Low and Mid bands and secondly a 4-pin symmetrical oscillator for High band operations including a band selector switch.

The output signal from the mixer is amplified via a SAW filter driver followed by variable gain amplifier stage in order to achieve a constant output level used for A/D conversion. All functions can be programmed with up to four different IC addresses. Also, the PLL connected to a 4-16 MHz reference crystal which is buffered on-chip, allows the setting of the tuner oscillator with a minimum step size of 20 kHz. A Lock flag will be set once the PLL is locked and communicated via the I2C/3-Wire bus.

The complete control setting of the IC is done by a microprocessor via the I2C/3-Wire bus. The device also has three output ports of which P2 can be configured as a programmable output voltage port.

2.1 Features

2.1.1 General

- Supply voltage range 3 to 5.5 V.
- Suitable for PAL, NTSC, SECAM, DVB-T/H/C, DAB, ISDB-T, ATSC and L-Band.
- Wideband and Narrow AGC detectors for tuner RF AGC
  – 5 programmable take-over points
  – 2 programmable time constants.
- Low phase noise.
- Full ESD protection.

2.1.2 Mixer/Oscillator

- High impedance mixer input (common emitter) for LOW band.
- Low impedance mixer input (common base) for MID band.
- Low impedance mixer input (common base) for HIGH band.
- 2 pin oscillator for LOW band.
- 2 pin oscillator for MID band.
- 4 pin oscillator for HIGH band.
- Oscillator for HIGH band divided by 3 available for MID band mixer.

2.1.3 SAW Filter Driver

- Symmetrical IF preamplifier with low output impedance able to drive a compensated SAW filter (500 Ω//40 pF).

2.1.4 IF AGC Amplifier

- Symmetrical variable gain IF output amplifier with low noise, high linearity, high dynamic range.

2.1.5 PLL

- 4 independent I^2C addresses, or 3-Wire bus mode.
- I^2C bus protocol compatible with 3.3 V and 5V micro-controllers up to 400 kHz.
- High voltage VCO tuning output.
- 3 PNP ports, one of them realized as programmable voltage output.
- 1 clock output for external DC/DC upconversion to generate the tuning supply voltage, may be used as NPN port.
- Stand-by programmable for functional blocks allows customized ramping.
- Internal LOW/MID/HIGH band switch.
- Lock-in flag.
- 4 to 16 MHz crystal oscillator with programmable output buffer.
- programmable reference divider ratios.
- 4 charge pump currents, programmable in 15 steps.

2.1.6 DAC outputs

- Open drain outputs, load resistors to Vcc, 5V or tuning supply voltage.
- Overvoltage protection for operation from tuning supply voltage.

2.1.7 IF switch and Loop through for tuner alignment

- 2 programmable switches to bypass the bandpass/SAW filter to facilitate the tuner pre-stage alignment.

2.2 Application

- The IC is suitable for PAL, NTSC, SECAM, DVB-T/H/C, DAB, ISDB-T, ATSC and L-Band tuners.
- The integrated RF AGC control has wide band detectors at the mixer inputs and a narrowband detector at the saw filter driver output.

2.2.1 Recommended band limits in MHz

Table 1 ATSC tuners

	RF input		Oscillator	
Band	**min.**	**max.**	**min.**	**max.**
LOW	55.25	157.25	101	203
MID	163.25	451.25	201	479
HIGH	457.25	861.25	503	907

Table 2 DVB-T and analog tuners

	RF input		Oscillator	
Band	**min.**	**max.**	**min.**	**max.**
LOW	48.25	154.25	87.15	193.15
MID	161.25	439.25	200.15	478.15
HIGH	447.25	863.25	486.15	902.15

Table 3 ISDB-T tuners

	RF input		Oscillator	
Band	**min.**	**max.**	**min.**	**max.**
LOW	93	167	150	224
MID	173	467	230	524
HIGH	473	767	530	824

Note: Tuning margin of 3 MHz not included.

3 Functional Description

3.1 Pin Configuration

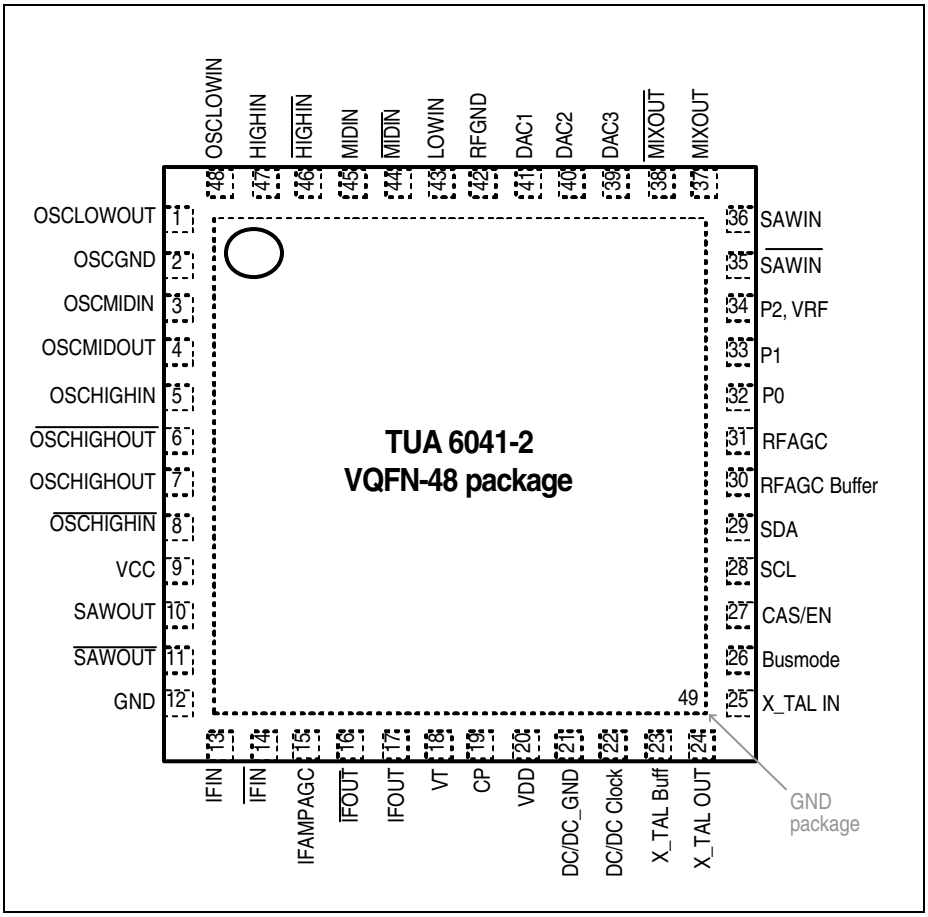
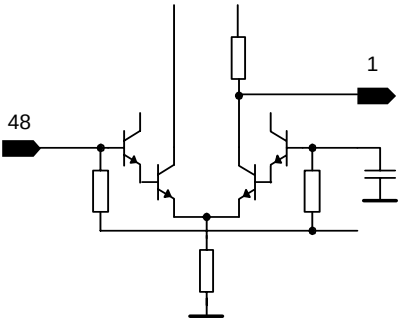
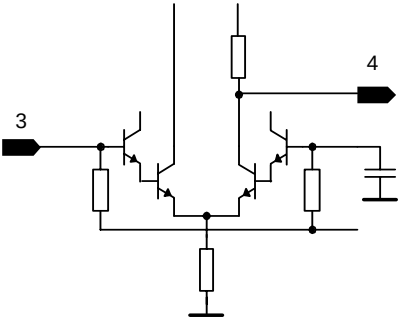
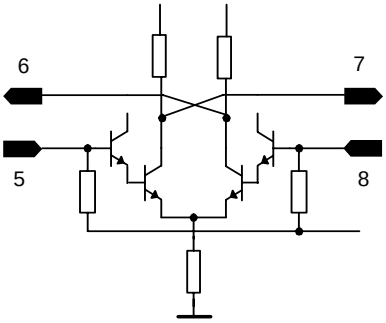
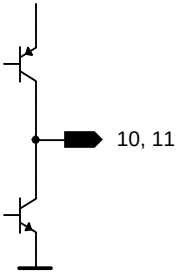
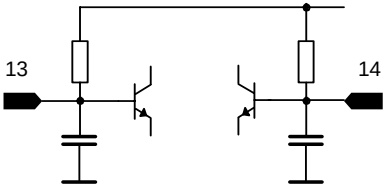


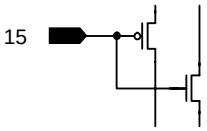
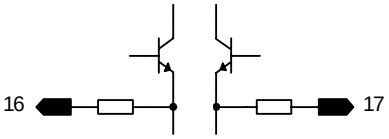
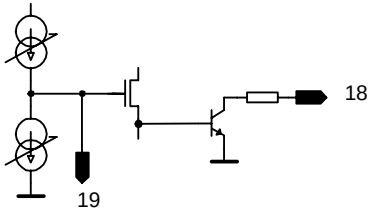
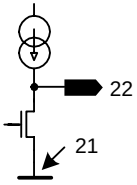
Figure 1 Pin Configuration TUA 6041-2 in VQFN-48 Package

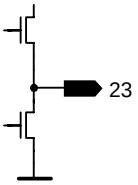
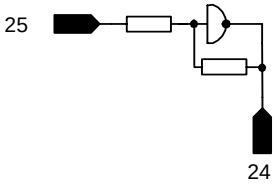
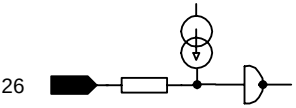
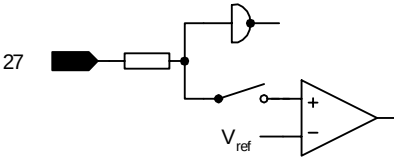
3.2 Pin Definition and Functions

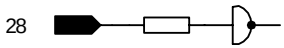
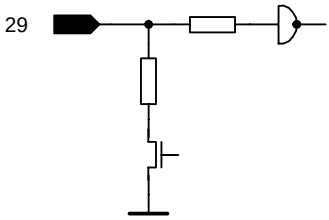
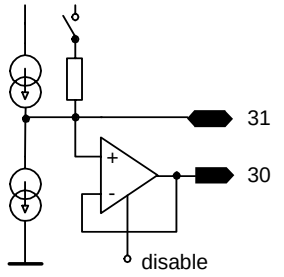
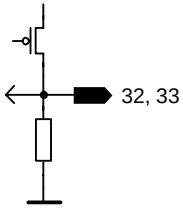
- Pin Definition and Functions

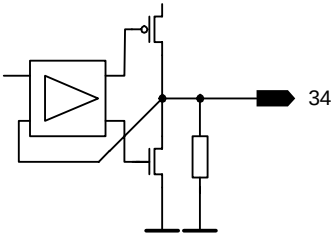
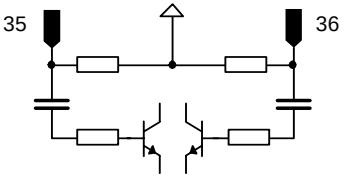
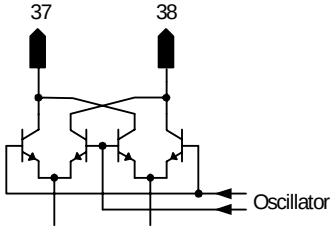
Pin No.	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 3.3V		
			LOW	MID	HIGH
48	OSCLOWIN		2.3 V		
1	OSCLOWOUT		1.8 V		
2	OSCGND	Oscillator ground	0.0 V	0.0 V	0.0 V
3	OSCMIDIN			2.3 V	
4	OSCMIDOUT			1.8 V	

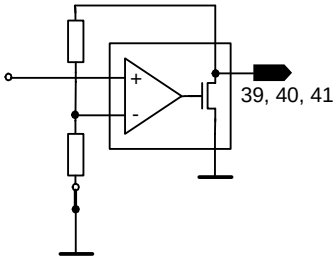
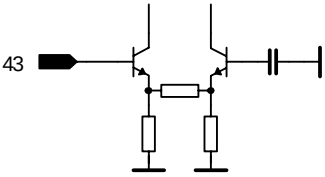
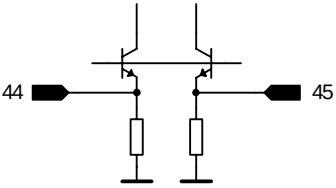
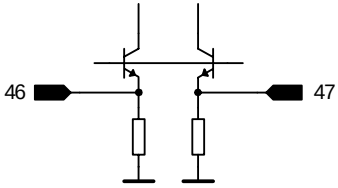
Pin No.	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 3.3V		
			LOW	MID	HIGH
5	OSCHIGHIN				2.3 V
6	OSCHIGOUT				2.25 V
7	OSCHIGOUT				2.25 V
8	OSCHIGHIN				2.3 V
9	VCC	Supply voltage	3.3 V	3.3 V	3.3 V
10	SAWOUT		1.65 V	1.65 V	1.65 V
11	SAWOUT		1.65 V	1.65 V	1.65 V
12	GND		0.0 V	0.0 V	0.0 V
13	IFIN		2.64 V	2.64 V	2.64 V
14	IFIN		2.64 V	2.64 V	2.64 V

Pin No.	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 3.3V		
			LOW	MID	HIGH
15	IFAMPAGC		n.a.	n.a.	n.a.
16	IFOUT		1.6 V	1.6 V	1.6 V
17	IFOUT		1.6 V	1.6 V	1.6 V
18	VT		VT	VT	VT
19	CP		1.7 V	1.7 V	1.7 V
20	VDD	Supply voltage	3.3 V	3.3 V	3.3 V
21	DC/DC_GND		0.0 V	0.0 V	0.0 V
22	DC/DC Clock		n.a.	n.a.	n.a.

Pin No.	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 3.3V		
			LOW	MID	HIGH
23	XTAL Buffer				
24	XTAL Out		0.9 V	0.9 V	0.9 V
25	XTAL In		0.9 V	0.9 V	0.9 V
26	Busmode		n.a.	n.a.	n.a.
27	CAS/EN		n.a.	n.a.	n.a.

Pin No.	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 3.3V		
			LOW	MID	HIGH
28	SCL		n.a.	n.a.	n.a.
29	SDA		n.a.	n.a.	n.a.
30	RFAGC Buffer		3.2 V	3.2 V	3.2 V
31	RFAGC		3.2 V	3.2 V	3.2 V
32	P0		0 V or V_{CC}-V_{CE}	0 V or V_{CC}-V_{CE}	0 V or V_{CC}-V_{CE}
33	P1		0 V or V_{CC}-V_{CE}	0 V or V_{CC}-V_{CE}	0 V or V_{CC}-V_{CE}

Pin No.	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 3.3V		
			LOW	MID	HIGH
34	P2, VRF		VRF	VRF	VRF
35	SAWIN		V_{CC}	V_{CC}	V_{CC}
36	SAWIN		V_{CC}	V_{CC}	V_{CC}
37	MIXOUT		V_{CC}	V_{CC}	V_{CC}
38	MIXOUT		V_{CC}	V_{CC}	V_{CC}

Pin No.	Symbol	Equivalent I/O Schematic	Average DC voltage at V_{CC} = 3.3V		
			LOW	MID	HIGH
39	DAC3		V_{DAC3}	V_{DAC3}	V_{DAC3}
40	DAC2		V_{DAC2}	V_{DAC2}	V_{DAC2}
41	DAC1		V_{DAC1}	V_{DAC1}	V_{DAC1}
42	RFGND	IF ground	0.0 V	0.0 V	0.0 V
43	LOWIN		2		
44	MIDIN			1	
45	MIDIN			1	
46	HIGHIN				1
47	HIGHIN				1
49	GND package	Exposed pad ground (Die pad)	0.0 V	0.0 V	0.0 V

3.3 Functional Block Diagram

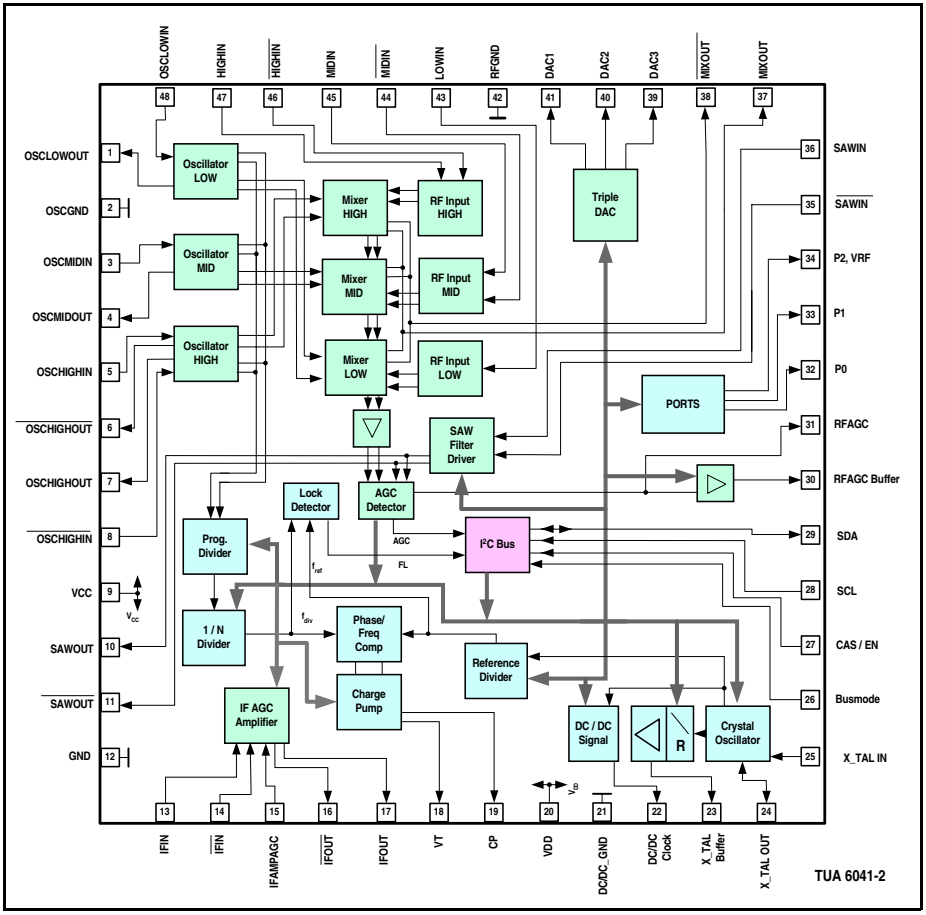


Figure 2 Functional Block Diagram TUA 6041-2 in VQFN-48 package

3.4 Circuit Description

3.4.1 Mixer-Oscillator-block, SAW filter driver

The mixer-oscillator block includes three balanced mixers (one mixer with an unbalanced high-impedance input and two mixers with a balanced low-impedance input), two 2-pin asymmetrical oscillators for the LOW and the MID band, one 4-pin symmetrical oscillator for the HIGH band, a reference voltage, and a band switch.

Filters between tuner input and IC separate the TV frequency signals into three bands. The band switching in the tuner front-end is done by using three PNP port outputs. In the selected band, the signal passes through a tuner input stage with a MOSFET amplifier, a double-tuned bandpass filter and is finally fed to the mixer input of the IC. The impedance of the mixer at LOW band has high ohmic, while MID or HIGH band has a low ohmic input. The input signal is mixed there with the signal from the activated on chip oscillator to the IF frequency.

The IF is filtered by means of an external SAW filter (Surface Acoustic Waves filter) in between the 2 mixer output pins and the 2 input pins of the following SAW filter driver. The SAW filter driver has a low output impedance to drive the SAW filter directly.

3.4.2 RF AGC

The RF AGC stage combines a wide band and a narrow band detection. The wide band detector (WB) detects the input signal directly at the RF input for each band. The narrow band detector (NB) detects the level of the SAW filter driver output signal. If both detected levels are below the RF AGC take-over points, a external capacity will be charged with the source current of 300 nA or 9 µA (release current). If one of the detected levels is above the RF AGC take-over points, the external capacity will be discharged with the sink current of 100 µA (attack current). The integrated current generates an AGC voltage for gain control of the tuners input transistors. The AGC take-over and the time constant are selectable by the I^2C bus as shown in **Table 17 "Subaddress 03H, AGC Control and IF Signal Processing Control" on Page 53**.

An integrated RF AGC buffer allows to monitor the AGC voltage without any influence on the tuner gain control. This buffer can be disabled as shown in **Table 16 "Subaddress 02H, Reference Divider R and Crystal Oscillator Control" on Page 51**

3.4.3 IF AGC amplifier

Coming out of the SAW filter the IF signal is sent through a VGA (Variable Gain Amplifier) which will set the differential IF output signal to the desired level (preferably 1 Vpp). The gain of the VGA is determined by the DC-voltage at pin IFAMPAGC

3.4.4 PLL block, XTAL oscillator

The VCO frequency f_{OSC} is stabilized by a digital CMOS PLL (Phase Locked Loop, Frequency Synthesizer). The oscillator signal is internally DC-coupled as a differential signal to the programmable divider input. The signal subsequently passes through a programmable divider (N) and then the divided VCO signal:

$$f_{div} = \frac{f_{OSC}}{N}, (N = 240 \ldots 65535)$$

is compared in a digital frequency/phase detector (PD, frequency detector) with a programmable reference frequency:

$$f_{ref} = \frac{f_{XTAL}}{R}, (R = 2 \ldots 1023)$$

which is derived from a quartz reference f_{XTAL} divided by a programmable reference divider (R).

The phase detector has a linear operating range without a dead zone for very small phase deviations. A programmable ABL pulse width (Anti BackLash) works against the delay of the charge pump cell. The selectable ABL pulse width values have been implemented for test purpose only and have no performance effects.

The phase detector has two outputs (up & down) that drive two current sources of opposite polarity as charge pump (CP). If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the positive current source (I_{source}) pulses for the duration of the phase difference. In the reverse case the negative current source (I_{sink}) pulses. If the two signals are in phase (PLL is locked), the integrated charge pump current is approximately zero. In case of active closed loop control the charge pump provides programmable output current drive capability to optimize the loop requirements. The charge pump currents are programmable from 0 to 1.125 mA in steps of 75 µA.

The PLL contains an integrated lock detector. A lock-in flag is set when the loop is locked. It can be read by the processor via the common I^2C/3-Wire bus.

The crystal oscillator (XTAL) is an unbalanced Pierce oscillator which operates in parallel resonance with quartz crystals from 4...16 MHz. By programming it's possible to pass the oscillator frequency f_{XTAL} through a divider stage to a buffered output pin or to use an external quartz clock for the reference oscillator via a switchable preamplifier for test purpose only.

3.4.5 Bus Interface

The programming of the CMOS frequency synthesizer is done via a combined serial I^2C/3-Wire bus interface. The choice of the desired bus is made by a bus mode select signal at pin BUSMODE.

In I^2C-bus mode four different chip addresses can be set by appropriate DC levels at pin CAS (Chip Address Select), while in 3-Wire mode the chip is addressed by a low active enable signal at pin EN.

The content of the bus telegram (serial data format) is controlled by software programming and assigned to the registers of the functional units according to the several sub addresses. The most significant bit (MSB) of the data protocol is shifted in first.

The clock is generated by the processor (input pin SCL/Clock), while pin SDA/Data functions as an input or an output (open drain, external pull-up resistor) depending on the direction of the data (write or read mode). Both inputs have schmitt-trigger circuits with hysteresis and furthermore a low-pass characteristic, which suppress a certain noise level on the bus lines and enhance so the noise immunity of the combi-bus.

A detailed description of the chip address organization in I^2C-mode as well as the used sub addresses of the data registers is given in **chapter 5.2 "Bus Interface" on page 42** - and the programmable I^2C/3-Wire bus data format is shown in **chapter 5.3 "Bus Data Format" on page 44**.

3.4.6 DC/DC clock output

To drive a bipolar NPN switching transistor of an external DC/DC converter directly, a programmable DC/DC clock generator is integrated. The clock frequency and the duty cycle of the DC/DC clock generator can be set over the I^2C/3-Wire bus as shown in **Table 18 "Subaddress 04H, DC-DC Converter" on Page 55**.

3.4.7 DAC

Three DACs for digital alignment with a control range up to 5 volt can be programmed in 256 steps as shown in **Table 19 "Subaddress 05H, DACs" on Page 56**. This voltage is required for a automatic alignment of the tuner prestage filters as illustrated in **Figure 4 "Tuner application block diagram" on Page 26**.

3.4.8 Power-on Reset, Stand-by Condition

While applying the supply voltage, integrated power-on reset circuits ensure a defined state after initial power-up. The required programming data will be set to default values.

When V_{CC} fall below approximately 1.2 V (typ.) the power-on resets go active and tie all write data registers to their power-on defaults (= power-down reset). While power-on reset is active no programming is possible.

The power-on flags (POFx) are set at power-on and when V_{VCCx} falls below appr. 1.2 V (typ.). They will be reset at the end of a READ operation of the status register.

By programmable stand-by control bits it's possible to reduce the current consumption of the IC up to 99%. In the full stand-by mode only bus interface is staying active and the

current consumption is reduced below 200 µA. After power-on reset only bus interface and XTAL-oscillator with bandgap are active and the current consumption is about 2.6 mA (typ.).

3.4.9 IF switch, Loop thru

For the alignment procedure of the tuner module two programmable switches are integrated to bypass the bandpass, the SAW driver and the SAW filter. The first switch called “IF switch” can switch between the mixer output signal and the bandpass output signal. The second switch called “Loop thru” can switch between the signal after the first stage of the IF AGC amplifier and the SAW filter output signal.

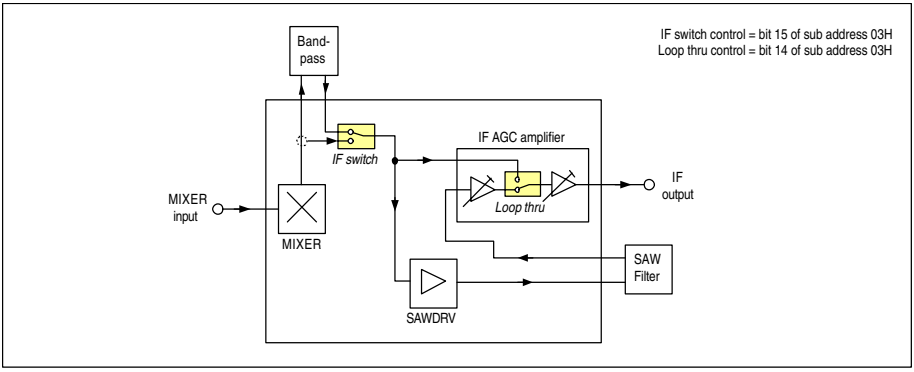


Figure 3 Functional Block Diagram of IF switch and Loop thru

4 Applications

4.1 Tuner application block diagram

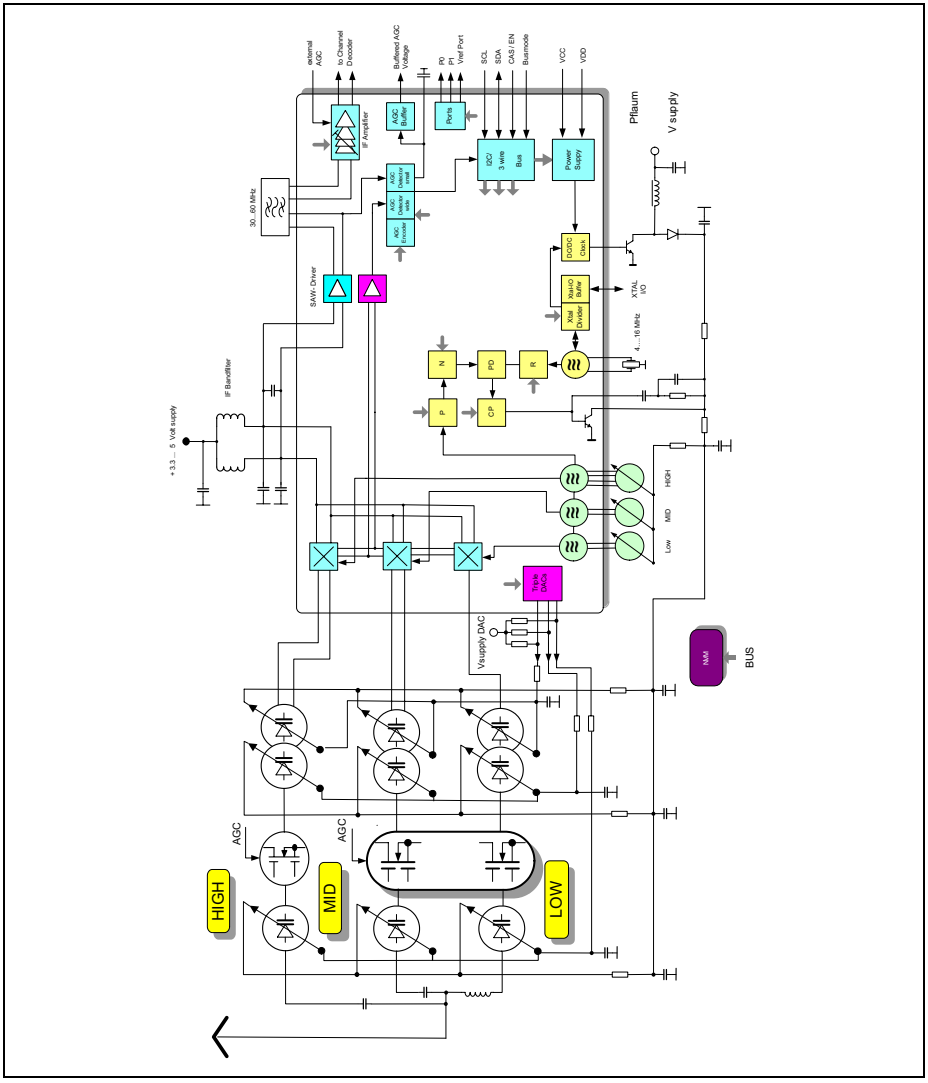


Figure 4 Tuner application block diagram

4.2 Application circuit for hybrid application

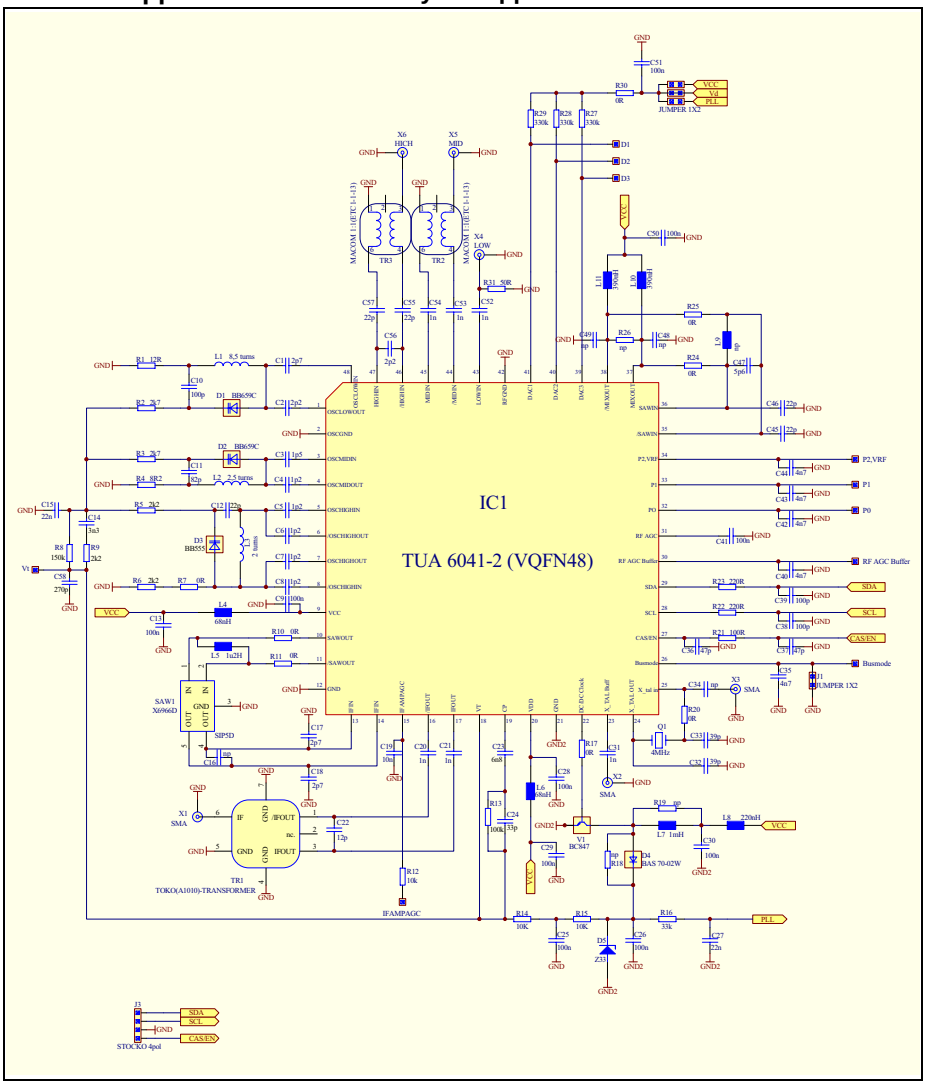


Figure 5 Circuit diagram for hybrid application (DVB-T / PAL)

4.3 Application circuit for L-Band application

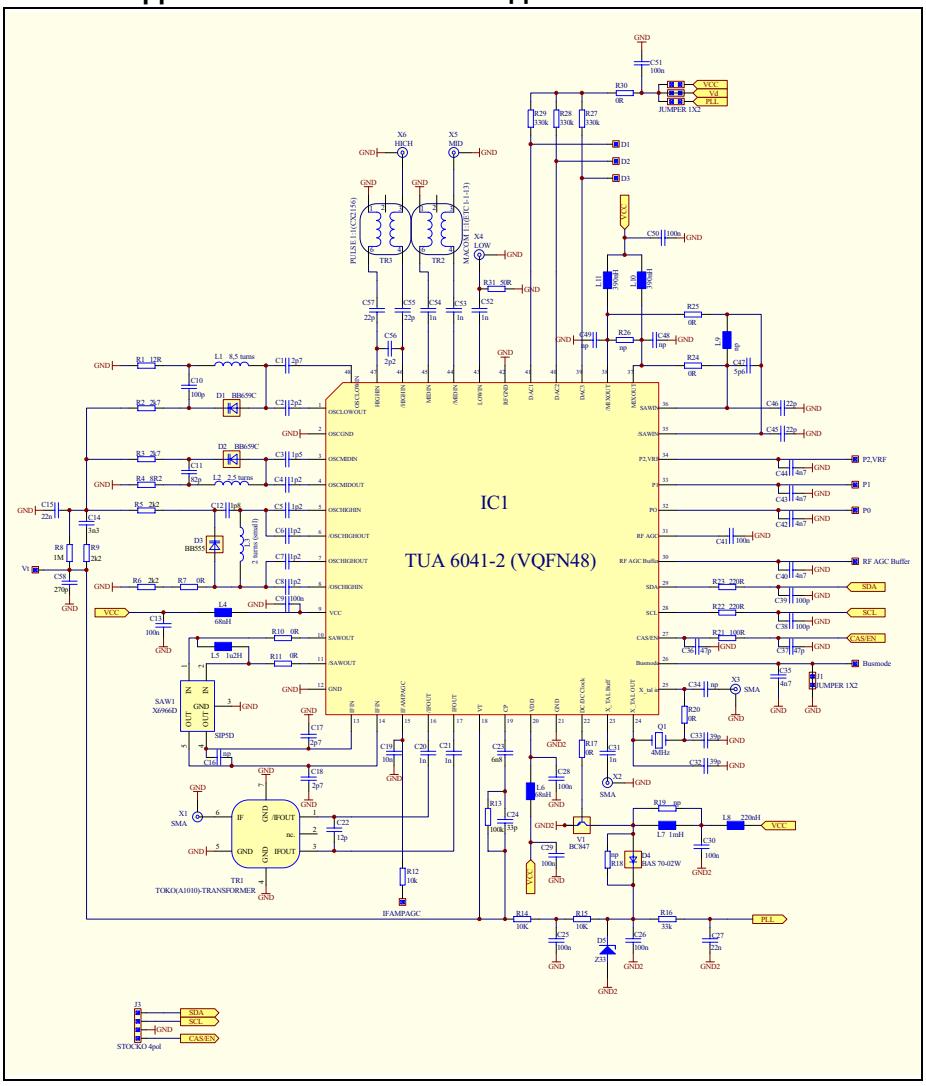


Figure 6 Circuit diagram for L-Band application

5 Reference

5.1 Electrical Data

5.1.1 Absolute Maximum Ratings

Attention: The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Table 4 Absolute Maximum Ratings

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
1.	Supply voltage	V_{CC}	-0.3	5.5	V	
2.	Ambient temperature	T_A	-40	+85	°C	exposed GND pad soldered
3.	Junction temperature	T_J	-40	+125	°C	
4.	Storage temperature	T_{Stg}	-40	+125	°C	
5.	Thermal resistance junction to ambient	R_{THJA}		39	K/W	exposed GND pad soldered
PLL						
6.	CP	V_{CP}	-0.3	3	V	
7.		I_{CP}		1	mA	
8.	Bus input/output SDA	V_{SDA}	-0.3	5.5	V	
9.	Bus output current SDA	$I_{SDA(L)}$		10	mA	open drain
10.	Bus input SCL	V_{SCL}	-0.3	5.5	V	
11.	Chip address switch AS	V_{AS}	-0.3	5.5	V	
12.	VCO tuning output (loop filter)	V_{VT}	-0.3	35	V	
13.	PMOS port output current of P0, P1	$I_{P(L)}$	-10	0	mA	open drain
14.	PMOS port output current of P2,VRF	$I_{P(L)}$	-2 -10	2 0	mA mA	analog voltage digital switch
15.	Total port output current of PMOS ports	$\Sigma I_{P(L)}$	-20	0	mA	t_{max} = 0.1 s at 5.5 V

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
16.	DC/DC output current	$I_{DC/DC}$		20	mA	
17.	DAC output current	I_{DAC}		5	mA	
Mixer-Oscillator						
18.	Mix inputs LOW band	V_{LOW}	-0.3	3	V	
19.	Mix inputs MID/HIGH band	$V_{MID/HIGH}$		2	V	
20.		$I_{MID/HIGH}$	-5	6	mA	
21.	VCO base voltage	V_B	-0.3	3	V	LOW, MID and HIGH band oscillators
22.	VCO collector voltage	V_C		5.5	V	LOW, MID and HIGH band oscillators
23.	Voltage on all other inputs, outputs, except GNDs	V_{max}	-0.3	V_{CC}	V	
ESD-Protection						
24.	all pins	V_{ESD}		2	kV	

5.1.2 Operating Range

Table 5 Operating Range

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
1.	Supply voltage	V_{CC}	+3.0	+5.5	V	nominal 3.3 V
2.	Ambient temperature	T_A	-20	+85	°C	exposed GND pad soldered
3.	Programmable divider factor	N	240	65535		
4.	LOW mixer input frequency range	f_{MIXL}	30	200	MHz	

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
5.	MID band mixer input frequency range	f_{MIXM}	130	500	MHz	
6.	HIGH band mixer input frequency range	f_{MIXH}	350	1500	MHz	
7.	LOW oscillator frequency range	f_{OL}	65	250	MHz	
8.	MID band oscillator frequency range	f_{OM}	165	530	MHz	
9.	HIGH band oscillator frequency range	f_{OH}	400	1550	MHz	

5.1.3 AC/DC Characteristics

Table 6 AC/DC Characteristics, T_A = 25°C, V_{CC} = 3.3V

#	Parameter[1)]	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
Supply								
10.	Current consumption in active mode	I_{VCC}		39		mA	VGA V1,V0=11, SAW S1,S0=11	
11.				47		mA	VGA V1,V0=10, SAW S1,S0=10	
12.				54		mA	VGA V1,V0=01, SAW S1,S0=01	
13.				64		mA	VGA V1,V0=00, SAW S1,S0=00	
14.		I_{MIX}		7		mA	Mixer current	
15.		I_{VDD}		8		mA	Digital part	

#	Parameter[1)]	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
16.	Current consumption in stand-by mode	I_{stby}		2.6		mA	bias, bus-interface and crystal oscillator active	
17.				170		µA	full standby IIC mode	
18.				7		µA	full standby 3-wire mode	
Digital Part								
PLL								
Crystal oscillator connections XTAL								
19.	Crystal frequency	f_{XTAL}	3.2	4.0	16	MHz		
20.	Crystal resistance	R_{XTAL}			270	Ω	4 MHz, 2x39pF	
21.					90	Ω	16 MHz, 2x18pF	
22.	Crystal oscillator transconductance	$g_{m,XTAL}$		-850	-600	µA/V	V_{OUT} = 0.9V V_{IN} = 0.8 to 1.0V	
23.	Oscillator impedance	$Y_{XTALOSC}$		-150		µA/V	4 MHz, 2x39pF	
24.				-200		µA/V	16 MHz, 2x18pF	
25.	Buffer output frequency	f_{XTALIO}	0.4		16	MHz	Divider ratios 1, 2, 4, 8	
26.	XTAL Buffer output low voltage	V_{low}	0	50	100	mV		
27.	Buffer signal voltage	V_{AC}		200		mV_{pp}	XTAL3,XTAL2=0,1	
28.				400		mV_{pp}	XTAL3,XTAL2=1,0	
29.				800		mV_{pp}	XTAL3,XTAL2=1,1	
30.	External input signal voltage	V_{ACin}	1	3		V_{pp}	Amp off	
31.			50	200		mV_{pp}	Amp on	
Tuning voltage output VT (open collector)								
32.	Output voltage when the loop is closed, (test mode in normal operation)	V_{TL}	0.4		32.7	V		

#	Parameter[1)]	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
Ports								
33.	Standard Ports (PMOS)	I_{max}	-10			mA		
34.	Output saturation voltage	V_{max}		0.25	0.4	V		
35.	Voltage referred port	I_{max}	-2			mA		
36.	Voltage referred port	V_0 V_1 ... V_{26} V_{27}		0 0.1 2.6 2.7		V V V V		
DC/DC clock generator								
37.	Programmable high	T_{High}	1		127		Multiple of crystal oscillator period	
38.	Programmable low	T_{Low}	1		127		Multiple of crystal oscillator period	
39.	Output high current	I_{high}		250		µA	Functional Range 0-2V	
40.	Output low impedance	R_{low}		10		Ω		
DA converter for digital alignment								
41.	Resolution	Res		8		Bit		
42.	Output voltage	V_{outmin}	0	20	100	mV	$I_{supplyDAC}$= 1 mA	
43.	DC output voltage	V_{outmax}	4.9	5.2	5.5	V	$I_{supplyDAC}$= 50 µA	
44.	DC output current	I_{outmax}			1	mA		
45.	DC output step size	ΔV_{out}	0	20	40	mV		
46.	Output noise density	ND		350		nV/rt Hz	@10 kHz	
Analog Part without IF AGC								
LOW band mixer and SAW driver at power level S1,S0=10								
47.	RF frequency	f_{RF}	44.25		170.25	MHz	picture carrier[2)]	

#	Parameter[1)]	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
48.	Voltage gain	G_V	21	24	27	dB	f_{RF} = 48.25 MHz to 154.25 MHz see 5.6.1 on page 61	
49.	Noise figure	NF		8	10	dB	f_{RF} = 48.25 MHz to 154.25 MHz see 5.6.4 on page 62	
50.	SAWOUT output voltage causing 0.8% of crossmodulation in channel	V_o		111		dBµV	f_{RF} = 48.25 MHz to 154.25 MHz see 5.6.6 on page 63	
51.	Input IP3	IIP3		120		dBµV	f_{RF1} = 48.25 MHz, f_{RF2} = 49.25 MHz, $P_{RF1} = P_{RF2}$	
52.				120		dBµV	f_{RF1} = 154.25 MHz, f_{RF2} = 155.25 MHz, $P_{RF1} = P_{RF2}$	
53.	SAWOUT output voltage causing 1 dB compression	V_o		125		dBµV	f_{RF} = 48.25 MHz to 154.25 MHz	
54.	Local oscillator FM caused by I^2C communication	FM_{I2C}			2.12	kHz	f_{RF} = 154.25 MHz[3)]	
55.	(N+5) - 1 MHz pulling	N+5 - 1 MHz	77	80		dBµV	f_{RFw} = 69.25 MHz, f_{OSC} = 108.15 MHz, f_{RFu} = 108.25 MHz[4)]	
56.	Input impedance $Z_i = (R_p \parallel 1/j\omega C_p)$	R_p		1		kΩ	parallel equivalent circuit at 100 MHz[5)]	
57.		C_p		2		pF		
Mid band mixer and SAW driver at power level S1,S0=10								
58.	RF frequency	f_{RF}	154.25		454.25	MHz	picture carrier[2)]	
59.	Voltage gain	G_V	31	34	37	dB	f_{RF} = 161.25 MHz to 439.25 MHz see 5.6.2 on page 61	

#	Parameter[1)]	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
60.	Noise figure (not corrected for image)	NF		6	8	dB	f_{RF} = 161.25 MHz to 439.25 MHz see 5.6.5 on page 63	
61.	SAWOUT output voltage causing 0.8% of crossmodulation in channel	V_o		110		dBµV	f_{RF} = 161.25 MHz to 439.25 MHz see 5.6.7 on page 64	
62.	Input IP3	IIP3		110		dBµV	f_{RF1} = 161.25 MHz, f_{RF2} = 162.25 MHz, $P_{RF1} = P_{RF2}$	
63.				108		dBµV	f_{RF1} = 439.25 MHz, f_{RF2} = 440.25 MHz, $P_{RF1} = P_{RF2}$	
64.	SAWOUT output voltage causing 1 dB compression	V_o		125		dBµV	f_{RF} = 161.25 MHz to 439.25 MHz	
65.	Local oscillator FM caused by I^2C communication	FM_{I2C}			2.12	kHz	f_{RF} = 439.25 MHz[3)]	
66.	(N+5) - 1 MHz pulling	N+5 - 1 MHz	77	80		dBµV	f_{RFw} = 359.25 MHz, f_{OSC} = 398.15 MHz, f_{RFu} = 398.25 MHz[4)]	
67.	Input impedance $Z_i = (R_s + j\omega L_s)$	R_s		35		Ω	f_{RF} = 161.25 MHz to 439.25 MHz[5)]	
68.		L_s		8		nH		
HIGH band mixer and SAW driver at power level S1,S0=10								
69.	RF frequency	f_{RF}	399.25		863.25	MHz	picture carrier[2)]	
70.	Voltage gain	G_V	31	34	37	dB	f_{RF} = 447.25 MHz to 863.25 MHz see 5.6.2 on page 61	
71.	Noise figure (not corrected for image)	NF		6	8	dB	f_{RF} = 447.25 MHz to 863.25 MHz see 5.6.5 on page 63	

#	Parameter[1]	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
72.	SAWOUT output voltage causing 0.8% of crossmodulation in channel	V_o		110		dBµV	f_{RF} = 447.25 MHz to 863.25 MHz see 5.6.7 on page 64	
73.	Input IP3	IIP3		106		dBµV	f_{RF1} = 447.25 MHz, f_{RF2} = 448.25 MHz, $P_{RF1} = P_{RF2}$	
74.				108		dBµV	f_{RF1} = 863.25 MHz, f_{RF2} = 864.25 MHz, $P_{RF1} = P_{RF2}$	
75.	SAWOUT output voltage causing 1 dB compression	V_o		125		dBµV	f_{RF} = 447.25 MHz to 863.25 MHz	
76.	Local oscillator FM caused by I^2C communication	FM_{I2C}			2.12	kHz	f_{RF} = 863.25 MHz[3]	
77.	(N+5) - 1 MHz pulling	N+5 - 1 MHz	77	80		dBµV	f_{RFw} = 823.25 MHz, f_{OSC} = 862.15 MHz, f_{RFu} = 862.25 MHz[4]	
78.	Input impedance $Z_i = (R_s + j\omega L_s)$	R_s		35		Ω	f_{RF} = 447.25 MHz to 863.25 MHz[5]	
79.		L_s		8		nH		
HIGH band mixer and SAW driver in L-Band application (see 4.3 on page 28)								
80.	RF frequency	f_{RF}	1452		1492	MHz	picture carrier[2]	
81.	Voltage gain	G_V	29	32	35	dB	f_{RF} = 1452 MHz to 1492 MHz see 5.6.2 on page 61	
82.	Noise figure (not corrected for image)	NF		8	10	dB	f_{RF} = 1452 MHz to 1492 MHz see 5.6.5 on page 63	
LOW band oscillator								
83.	Oscillator frequency	f_{OSC}	80		210	MHz	[6]	

#	Parameter[1)]	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
84.	Phase noise, carrier to noise sideband	Φ_{OSC}		-84	-77	dBc/ Hz	±1 kHz frequency offset, wide loop, worst case in the frequency range	
85.				-92	-88	dBc/ Hz	±10 kHz frequency offset, narrow loop, worst case in the frequency range	
86.				-112	-106	dBc/ Hz	±100 kHz frequency offset, worst case in the frequency range	
87.	Ripple susceptibility of V_{CC}	RSC		-22		dBc	V_{Ripple} = 20 mVpp, f_{Ripple} = 1 kHz[7)]	
88.				-50		dBc	V_{Ripple} = 20 mVpp, f_{Ripple} = 100 kHz[7)]	
MID band oscillator								
89.	Oscillator frequency	f_{OSC}	201		493	MHz	[6)]	
90.	Phase noise, carrier to noise sideband	Φ_{OSC}		-82	-75	dBc/ Hz	±1 kHz frequency offset, wide loop, worst case in the frequency range	
91.				-92	-88	dBc/ Hz	±10 kHz frequency offset, narrow loop, worst case in the frequency range	
92.				-112	-106	dBc/ Hz	±100 kHz frequency offset, worst case in the frequency range	
93.	Ripple susceptibility of V_{CC}	RSC		-25		dBc	V_{Ripple} = 20 mVpp, f_{Ripple} = 1 kHz[7)]	
94.				-55		dBc	V_{Ripple} = 20 mVpp, f_{Ripple} = 100 kHz[7)]	

#	Parameter[1)]	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
HIGH band oscillator								
95.	Oscillator frequency	f_{OSC}	435		905	MHz	[6)]	
96.	Phase noise, carrier to noise sideband	Φ_{OSC}		-80	-73	dBc/ Hz	±1 kHz frequency offset, wide loop, worst case in the frequency range	
97.				-90	-86	dBc/ Hz	±10 kHz frequency offset, narrow loop, worst case in the frequency range	
98.				-110	-106	dBc/ Hz	±100 kHz frequency offset, worst case in the frequency range	
99.	Ripple susceptibility of V_{CC}	RSC		-30		dBc	V_{Ripple} = 20 mVpp, f_{Ripple} = 1 kHz[7)]	
100.				-55		dBc	V_{Ripple} = 20 mVpp, f_{Ripple} = 100 kHz[7)]	
HIGH band oscillator in L-Band application (see 4.3 on page 28)								
101.	Oscillator frequency	f_{OSC}	1488		1528	MHz	[6)]	
102.	Phase noise, carrier to noise sideband			-85	-80	dBc/ Hz	±10 kHz frequency offset, narrow loop, f_{RF} = 1452 MHz to 1492 MHz	
SAW driver								
103.	Voltage gain	G_V		20		dB	f_{IF} = 36 MHz to 54 MHz	
104.	Input impedance $Z_i = (R_p \parallel 1/j\omega C_p)$	R_p		450		Ω	parallel equivalent circuit at 36 MHz[5)]	
105.		C_p		5		pF		
106.	Output impedance $Z_o = (R_s + j\omega L_s)$	R_S		65		Ω	series equivalent circuit at 36 MHz[5)]	
107.		L_S		20		nH		
Rejection at the SAW driver output								

#	Parameter[1)]	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
108.	Level of divider interferences in the IF signal	INT_{DIV}		-66	-60	dBc	V_{OUT} = 100 dBµV[8)]	
109.	Crystal oscillator interferences rejection	INT_{XTAL}		-66	-60	dBc	V_{OUT} = 100 dBµV[9)]	
110.	Reference frequency rejection	INT_{REF}		-66	-60	dBc	V_{OUT} = 100 dBµV[10)]	
111.	Channel S02 beat	INT_{S02}		-60	-57	dBc	f_{RFpix} = 76.25 MHz, V_{RFpix} = 80 dBµV[11)]	
RF AGC output								
112.	RF AGC take-over point wide band (RF input)	$AGC_{TOP\ wide}$	87 77		99 89	dBµV	LOW Band MID, HIGH Band	
113.	RF AGC take-over point narrow band (SAWOUT)	$AGC_{TOP\ narrow}$	103		115	dBµV		
114.	Source current 1	$I_{AGCfast}$		9.0		µA		
115.	Source current 2	$I_{AGCslow}$		300		nA		
116.	Peak sink to ground	$I_{AGCpeak}$		100		µA		
117.	RF AGC leakage current	AGC_{LEAK}	-50		50	nA	$0 < V_{AGC} < V_{CC}$	
118.	RF AGC output voltage	V_{AGCmax}	V_{CC}-0.25		V_{CC}	V	maximum level	
119.		V_{AGCmin}	0		0.25	V	minimum level	
120.	RF voltage range to switch the AGC from active to inactive mode	AGC_{SLIP}			0.5	dB		
RF AGC buffer output								
121.	RF AGC buffer output current	I_{max}			2	mA		
122.	Saturation voltage low	V_{Sat_low}		100		mV	I_{load} = 1mA	
123.				200		mV	I_{load} = 2mA	

#	Parameter[1)]	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
124.	Saturation voltage high	V_{Sat_high}		100		mV	I_{load} = 1mA	
125.				200		mV	I_{load} = 2mA	
126.	RF AGC Buffer output voltage	AGC_{OFF}		0		V	Power down	
IF amplifier								
127.	Voltage gain	G_{max}		65		dB	$V_{IFAGC} \geq 2.5$ V	
128.		G_{min}		9		dB	$V_{IFAGC} \leq 0.2$ V	
129.	Maximum IF input level	$V_{IF/\overline{IF}}$		102		dBµV	min. gain, $f_{IF/\overline{IF}}$ = 36 MHz (sine), V_{IFAGC} = 0.2 V, $V_{OUT/\overline{OUT}}$ = 1 V_{pp}	
130.	Minimum IF input level	$V_{IF/\overline{IF}}$		46			max. gain, $f_{IF/\overline{IF}}$ = 36 MHz (sine), V_{IFAGC} = 2.5 V, $V_{OUT/\overline{OUT}}$ = 1 V_{pp}	
131.	Input impedance	$R_{IF/\overline{IF}}$		2		kΩ	$f_{IF/\overline{IF}}$ = 36 MHz, parallel equivalent circuit[5)]	
132.		$C_{IF/\overline{IF}}$		1.5		pF		
133.	Low end cutoff frequency (-1 dB)	f_L			25	MHz	$V_{IF/\overline{IF}}$ = 60 dBµV, $R_{LOAD} \geq 5$ kΩ, $C_{LOAD} \leq 1.5$ pF, $V_{OUT/\overline{OUT}}$ = 1 V_{pp} at $f_{IF/\overline{IF}}$ = 36 MHz (sine)	
134.	High end cutoff frequency (-1 dB)	f_H	65			MHz		
135.	Intermodulation V1,V0 = 00 (5.0mA) V1,V0 = 01 (3.6mA) V1,V0 = 10 (2.1mA)	 C/IM3 C/IM3 C/IM3		 -59 -58 -56	 -50 -50 -50	 dBc dBc dBc	$f_{IF/\overline{IF}1}$ = 37 MHz, $f_{IF/\overline{IF}2}$ = 38 MHz, $V_{IF/\overline{IF}1}$ = 90 dBµV, $V_{IF/\overline{IF}2}$ = 90 dBµV R_{LOAD}=1 kΩ, C_{LOAD} = 10pF, $V_{OUT/\overline{OUT}}$ = 1 V_{pp}	

#	Parameter[1)]	Symbol	Limit Values			Unit	Test Conditions	■
			min.	typ.	max.			
136.	Intermodulation V1,V0 = 11 (1.1mA)	C/IM3		-56	-50	dBc	$f_{IF/\overline{IF}1}$ = 37 MHz, $f_{IF/\overline{IF}2}$ = 38 MHz, $V_{IF/\overline{IF}1}$ = 90 dBµV, $V_{IF/\overline{IF}2}$ = 90 dBµV R_{LOAD} ≥ 15 kΩ, C_{LOAD} = 1.5pF, $V_{OUT/\overline{OUT}}$ = 1 V_{pp}	
137.	Third order output intercept point V1,V0 = 00 (5.0mA)	OIP3		133		dBµV	$f_{IF/\overline{IF}1}$ = 37 MHz, $f_{IF/\overline{IF}2}$ = 38 MHz, $V_{IF/\overline{IF}1}$ = 90 dBµV, $V_{IF/\overline{IF}2}$ = 90 dBµV R_{LOAD} = 1 kΩ, C_{LOAD} =10 pF, $V_{OUT/\overline{OUT}}$ = 1 V_{pp}	
138.	Signal to noise ratio	SNR		43		dB	$f_{IF/\overline{IF}}$ = 36 MHz (sine), $V_{IF/\overline{IF}}$ = 60 dBµV, $V_{OUT/\overline{OUT}}$ = 1 V_{pp}, BW = 8 MHz	
139.	Noise figure			10		dB	max. gain	
140.	Output impedance	$R_{IF/\overline{IF}}$		90	150	Ω	$f_{OUT/\overline{OUT}}$ = 36 MHz, series equivalent circuit[5)]	
141.		$L_{IF/\overline{IF}}$		120		nH		

1) Values are referred to **Figure 4.2 "Application circuit for hybrid application" on Page 27** and f_{IF} = 36 MHz, unless stated otherwise.

2) The RF frequency range is defined by the oscillator frequency range and the intermediate frequency (IF).

3) Local oscillator FM modulation resulting from I^2C communication is measured at the IF output using a modulation analyzer with a peak to peak detector ((P_+ +P_-)/2) and a post detection filter 20 Hz - 100 kHz. The I^2C messages are sent to the tuner in such a way that the tuner is addressed but the content of the PLL registers are not altered. The refresh interval between each data set shall be 20 ms to 1s.

4) (N+5) -1 MHz is defined as the input level of channel N+5, at frequency 1 MHz lower, causing 100 kHz FM sidebands 30 dB below the wanted carrier.

5) Impedance measured with differential 2-port measurement at input or output. Input and output pins directly connected to measurement equipment with 50 Ω strip lines.

6) Limits are related to the tank circuit used in the application board. Frequency bands may be adjusted by the choice of external components.

7) The supply ripple susceptibility is a sideband measurement using a spectrum analyzer connected to the IF output. An unmodulated RF signal with a level of 80 dBµV is applied to the test board RF input. A sinewave signal with a defined frequency is superposed onto the supply voltage (see **Figure 16 "Ripple susceptibility measurement" on Page 64**). The specified value is the worst case in the frequency range.

8) This is the level of divider interferences close to the IF frequency. For example channel S3: f_{OSC} = 158.15 MHz, 1/4 f_{OSC} = 39.5375 MHz. The rejection has to be greater than 60 dB for an SAW driver output of 100 dBµV.

9) Crystal oscillator interference means the 4 MHz sidebands caused by the crystal oscillator. The rejection has to be greater than 60 dB for an SAW driver output of 100 dBµV.

10) The reference frequency rejection is the level of reference frequency sidebands (e.g. 62.5 kHz) related to the carrier. The rejection has to be greater than 60 dB for an SAW driver output of 100 dBµV.

11) Channel S02 beat is the interfering product of f_{RFpix}, f_{IF} and f_{OSC} of channel S02, f_{BEAT} = 37.35 MHz. The possible mechanisms are f_{OSC} - 2 x f_{IF} or 2 x f_{RFpix} - f_{OSC}.

5.2 Bus Interface

Table 7 Pin Function

Pin Designation	BUSMODE	SDA / Data	SCL / Clock	CAS / EN
Function	bus mode select	serial data	clock	I^2C: chip address select, 3-W: enable
I^2C mode	0	data in/out	clock in	four chip addresses 1)
3-Wire mode	1 or open			0: chip is addressed

1) **see Table 8 Chip Address Organization in I2C Mode on page 42**, **see Table 9 Address selection in I2C Mode on page 43**

Table 8 Chip Address Organization in I^2C Mode

Name	Byte	MSB	bit6	bit5	bit4	bit3	bit2	bit1	LSB
Write Mode									
Address Byte	ADB	1	1	0	0	0	MA1	MA0	R/W=0
Read Mode									
Address Byte	ADB	1	1	0	0	0	MA1	MA0	R/W=1

Table 9 Address selection in I²C Mode

			Chip Address (Hex)	
Voltage at pin CAS/EN	**MA1**	**MA0**	**Write Mode**	**Read Mode**
(0 to 0.1) x V_{VCCD}	0	0	C0	C1
open circuit or (0.2 to 0.3) x V_{VCCD}	0	1	C2	C3
(0.4 to 0.6) x V_{VCCD}	1	0	C4	C5
(0.9 to 1) x V_{VCCD}	1	1	C6	C7

Table 10 Sub Addresses of Write Data Registers

Function	Hex	MSB	S6	S5	S4	S3	S2	S1	LSB
Main Divider	00	0	0	0	0	0	0	0	0
Control bytes	01	0	0	0	0	0	0	0	1
Ref. Divider (R)	02	0	0	0	0	0	0	1	0
AGC control, IF signal processing control	03	0	0	0	0	0	0	1	1
DC-DC converter	04	0	0	0	0	0	1	0	0
DACs	05	0	0	0	0	0	1	0	1
Mode bytes, stand by, test	06	0	0	0	0	0	1	1	0

Table 11 Sub Addresses of Read Data Registers

Function	Hex	MSB	S6	S5	S4	S3	S2	S1	LSB
Status	80	1	0	0	0	0	0	0	0
Chip Code	8E	1	0	0	0	1	1	1	0
Revision Code	8F	1	0	0	0	1	1	1	1

5.3 Bus Data Format

Table 12 Bus Data Format

I²C-bus Write Mode		I²C-bus Read Mode		3W-bus Write Mode		3W-bus Read Mode	
Bit	**Function**	**Bit**	**Function**	**Bit**	**Function**	**Bit**	**Function**
STA		STA					
1	MSB	1	MSB				
1	chip address (Write)	1	chip address (Write)				
0		0					
0		0					
0		0					
MA0		MA0					
MA1		MA1					
0	LSB	0	LSB				
ACK		ACK					
S7	MSB	S7	MSB	S7	MSB	S7	MSB
S6	sub address (Write) 00H...06H	S6	sub address (Read) 80H, 8EH, 8FH	S6	sub address (Write) 00H...06H	S6	sub address (Read) 80H 8EH, 8FH
S5		S5		S5		S5	
S4		S4		S4		S4	
S3		S3		S3		S3	
S2		S2		S2		S2	
S1		S1		S1		S1	
S0	LSB	S0	LSB	S0	LSB	S0	LSB
ACK		ACK					
		STA	restart				
DX	MSB	1	MSB	DX	MSB	DX	MSB

I²C-bus Write Mode		I²C-bus Read Mode		3W-bus Write Mode		3W-bus Read Mode	
Bit	**Function**	**Bit**	**Function**	**Bit**	**Function**	**Bit**	**Function**
...	data in X...0 (X=7,15 or 23) [1]	1	chip address (Read)	...	data in X...0 (X=7,15 or 23)	...	data out X...0 (X=7 or 15)
D5		0		D5		D5	
D4		0		D4		D4	
D3		0		D3		D3	
D2		MA0		D2		D2	
D1		MA1		D1		D1	
D0	LSB	1	LSB	D0	LSB	D0	LSB
ACK		ACK					
STO		DX	MSB				
[1] after each byte an acknowledge is generated by TUA 6041. [2] after each byte an acknowledge is generated by the processor. TUA 6041 keeps data line high.		...	data out X...0 (X=7 or 15) [2]				
		D5					
		D4					
		D3					
		D2					
		D1					
		D0	LSB				
		1					
		STO					

STA: Start condition, STO: Stop condition, ACK: Acknowledge from TUA 6041.

5.4 Bus Timing

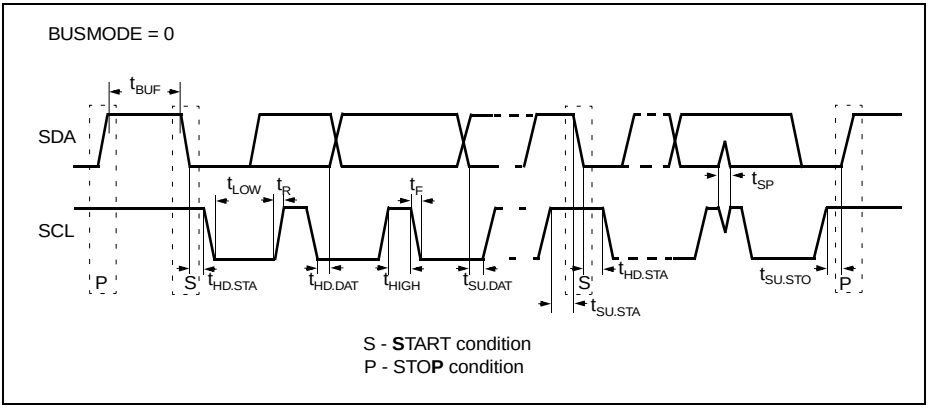


Figure 7 I²C Bus

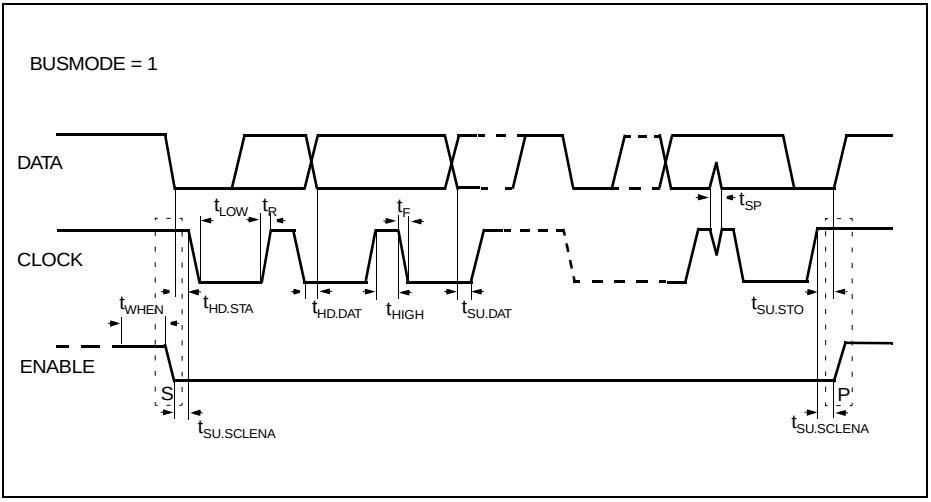


Figure 8 3-Wire Bus

Table 13 Bus Timing

#	Parameter	Symbol	Limit Values		Unit
			min.	max.	
1.	LOW level input voltage (SDA, SCL, CAS/EN, BUSMODE)	V_{IL}	-0.5	0.54	V
2.	HIGH level input voltage (SDA, SCL, CAS/EN, BUSMODE)	V_{IH}	1.26	5.5	V
3.	Hysteresis of Schmitt trigger inputs	V_{Hys}	0.15		V
4.	Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns
5.	LOW level output voltage (SDA), only I2C-bus at 3mA sink current at 6mA sink current	V_{OL}	0	 0.4 0.6	 V V
6.	Output fall time from $V_{IH\,min}$ to $V_{IL\,max}$ with a bus capacitance from 10pF to 400pF with up to 3mA sink current at V_{OL}	t_{OF}	$20+0.1C_b$ [1)]	250	ns
7.	SCL clock frequency	f_{SCL}	0	400	kHz
8.	Bus free time between a STOP and START condition [2)]	t_{BUF}	1.3	-	µs
9.	Hold time (repeated) START/ENABLE ON condition. After this period, the first clock pulse is generated.	$t_{HD.STA}$	0.6	-	µs
10.	LOW period of the SCL clock pulse	t_{LOW}	1.3	-	µs
11.	HIGH period of the SCL clock pulse	t_{HIGH}	0.6	-	µs
12.	Set-up time for a repeated START condition2)	$t_{SU.STA}$	0.6	-	µs
13.	Data hold time	$t_{HD.DAT}$	0	-	ns
14.	Data set-up time	$t_{SU.DAT}$	100	-	ns
15.	Rise time, fall time of SDA and SCL signals	t_R, t_F	$20+0.1C_b$ [1)]	300	ns
16.	Set-up time for STOP/ENABLE OFF condition	$t_{SU.STO}$	0.6	-	µs

#	Parameter	Symbol	Limit Values		Unit
			min.	max.	
17.	Setup time CAS/EN to SDA 3)	$t_{SU.ENASDA}$	0.6	-	µs
18.	Setup time SCL to CAS/EN	$t_{SU.SCLENA}$	0.6	-	µs
19.	H-pulse width (CAS/EN) for new data protocol 3)	t_{WHEN}	0.6	-	µs
20.	Capacitive load for each bus line	C_b	--	400	pF

1) C_b = capacitance of one bus line in pF.
Note that the maximum t_F for the SDA and SCL bus lines quoted in table above (300ns) is longer than the specified maximum t_{OF} for the output stages (250ns).This allows series protection resistors to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_F.

2) only for I^2C bus mode.

3) only for 3-Wire bus mode.

5.5 Data Byte Specification, Function and Defaults

5.5.1 Write Data Registers

Table 14 Subaddress 00H, Main Divider

Bit	Symbol	Bits	V	Function	Description	Defaults	
15	N15		2^{15}		Synthesizer N-counter programmable divider bits:	0	
14	N14		2^{14}			0	
13	N13		2^{13}			0	
12	N12		2^{12}			1	
11	N11		2^{11}			1	
10	N10		2^{10}		N = 2^{15} x N15 + ... + N0	1	Default divider ratio
9	N9		2^{9}			1	
8	N8		2^{8}			0	
7	N7		2^{7}			1	N = 7906[1)]
6	N6		2^{6}		N = 240 ... 65535	1	
5	N5		2^{5}			1	
4	N4		2^{4}			0	
3	N3		2^{3}			0	
2	N2		2^{2}	(internal A-counter A = 0 ... 15))		0	
1	N1		2^{1}			1	
0	N0		2^{0}			0	

1) Default: f_{RF} = 458MHz with f_{ref} = 62.5kHz, f_{IF} = 36.125MHz.

Table 15 Subaddress 01H, Control Bytes

Bit	Symbol	Bits	V	Function	Description	Defaults
15				not used	not used	0
		P2_4 ... P2_0		analog output		
14	P2_4	00000	0V	to 0V		1
13	P2_3	11011	2.7 V	to 2.7V		1
12	P2_2	111X1		on (Vcc)	standard port function	1
11	P2_1	11110		off (50k to GND)	standard port function	1
10	P2_0	11100		off (switch to GND)		1
9	P1	0		Portswitch	Port 1 current off	0
		1			Port 1 current on	
8	P0	0		Portswitch	Port 0 current off	0
		1			Port 0 current on	
7	BS1	BS1 BS0		Band switch selection		BS1 BS0
		0 0		Osc. 3 + Mix 3 on	HIGH	0 0
		0 1		Osc. 1 + Mix 1 on	LOW	
6	BS0	1 0		Osc. 2 + Mix 2 on	MID	
		1 1		Osc. 3 + Mix 2 on	MID, HIGH Osc. /3	
5	CP3			Synth. charge-pump current CP=CP0+CP1+CP2+CP3	600 µA	0
4	CP2				300 µA	0
3	CP1				150 µA	1
2	CP0				75 µA	0
1	ABL1	ABL1 ABL0		Anti-Backlash pulse width of phase detector PD	Pulse width	ABL1 ABL0
		0 0			2.2 ns	
		0 1			3.2 ns	0 1
0	ABL0	1 0			4.4 ns	
		1 1			5.6 ns	

Table 16 Subaddress 02H, Reference Divider R and Crystal Oscillator Control

Bit	Symbol	Bits		V	Function	Description	Defaults	
15					not used	not used	0	
14	RFAGCB_OFF				RF AGC buffer off	disable RF AGC buffer	0	
13	XTAL3	XTAL3	XTAL2		XTAL I/O control		XTAL3	XTAL2
		0	0			output off, input on		
		0	1			output 200 mVpp		
12	XTAL2	1	0			output 400 mVpp		
		1	1			output 800 mVpp	1	1
11	XTAL1	XTAL1	XTAL0		XTAL I/O control output mode XTAL3 OR XTAL2 =1		XTAL1	XTAL0
		0	0			Fout/1	0	0
		0	1			Fout/2		
		1	0			Fout/4		
		1	1			Fout/8		
10	XTAL0	XTAL1	XTAL0		XTAL I/O control input mode XTAL3=0 XTAL2=0		XTAL1	XTAL0
		0	0			XTAL_IN	0	0
		0	1			XTAL_IN		
		1	0			XTAL_Buff		
		1	1			XTAL_Buff+Amp		

Bit	Symbol	Bits	V	Function	Description	Defaults	
9	R9		2^9	Synthesizer R-counter	Synthesizer R-counter programmable divider bits: R= 2^9 x R9 + ... + R0 R = 2 ... 1023	0	
8	R8		2^8			0	
7	R7		2^7			0	Default div. ratio R=64
6	R6		2^6			1	
5	R5		2^5			0	
4	R4		2^4			0	
3	R3		2^3			0	
2	R2		2^2			0	
1	R1		2^1			0	
0	R0		2^0			0	

Table 17 Subaddress 03H, AGC Control and IF Signal Processing Control

Bit	Symbol	Bits			V	Function	Description	Defaults		
15	SW	0				IF Switch	normal mode	0		
		1					bypass mixer output tank			
14	LP	0				Loop thru control	normal mode	0		
		1					bypass SAW driver stage			
13	V1	V1	V0			VGA output power control	quiescent current of emitter follower per side	V1	V0	
12	V0	0	0				5.0 mA			
		0	1				3.6 mA			
		1	0				2.1 mA			
		1	1				1.1 mA	1	1	
11	S1	S1	S0			SAW driver power control	quiescent current for SAW driver stage per side	S1	S0	
10	S0	0	0				9.7 mA			
		0	1				6.7 mA			
		1	0				4.7 mA			
		1	1				2.1 mA	1	1	
9	ATC	0				RF-AGC time constant bit	0.3 µA	0		
		1					9.0 µA			
8	PU	0				RF-AGC time standby mode if RF-AGC in standby (Bit6 in register 06H is set)	tristate	0		
		1					200 kΩ pull-up			
7	AL2	AL2	AL1	AL0		NB-AGC control	NB-AGC take over point	AL2	AL1	AL0
6	AL1	0	0	0			don't use			

Bit	Symbol	Bits			V	Function	Description	Defaults		
5	AL0	0	0	1			115 dBµV			
		0	1	0			112 dBµV (default)	0	1	0
		0	1	1			don't use			
		1	0	0			109 dBµV			
		1	0	1			106 dBµV			
		1	1	0			103 dBµV			
		1	1	1			don't use			
4	NBE	0				Disable NB-AGC detector	Narrowband level detector active	0		
		1					Narrowband level detector does not affect AGC			
3	WBE	0				Disable WB-AGC detector	Wideband level detector active	0		
		1					Wideband level detector does not affect AGC			
2	WB2	WB 2	WB 1	WB 0		WB-AGC control	LOW/MID/HIGH take over point	WB 2	WB 1	WB 0
1	WB1	0	0	0			87 / 77 / 77 dBµV			
0	WB0	0	0	1			90 / 80 / 80 dBµV			
		0	1	0			93 / 83 / 83 dBµV	0	1	0
		0	1	1			96 / 86 / 86 dBµV			
		1	0	0			99 / 89 / 89 dBµV			
		1	0	1			don't use			
		1	1	0			don't use			
		1	1	1			don't use			

Table 18 Subaddress 04H, DC-DC Converter

Bit	Symbol	Bits	V	Function	Description	Defaults
15		1		Output HIGH	High current or tristate Output high time: High count register DCh=sum(DCh_i *2^i); 2^i =1 to 127 t_{High} = DCh / $f_{Crystal}$	0
14	DCh_6		2^6			0
13	DCh_5		2^5			0
12	DCh_4		2^4			0
11	DCh_3		2^3			0
10	DCh_2		2^2			1
9	DCh_1		2^1			0
8	DCh_0		2^0			0
7		1		Output LOW	If bit15 = 0, load count registers; Output low time: Low count register DCh=sum(DCl_i *2^i); 2^i =1 to 127 t_{Low} = DCl / $f_{Crystal}$	0
6	DCl_6		2^6			0
5	DCl_5		2^5			0
4	DCl_4		2^4			1
3	DCl_3		2^3			0
2	DCl_2		2^2			0
1	DCl_1		2^1			0
0	DCl_0		2^0			0

Default f_{DCDC} = 4 MHz / (4 +16) = 200 kHz, 20% duty cycle

Table 19 Subaddress 05H, DACs

Bit	Symbol	Bits	V	Function	Description	Defaults
23	DAC3_7		2^7	DAC 3	DAC output voltage: DAC register DAC3=sum(DAC3_i+2^i) VDAC3=5.2V*(DAC3+1)/256 accuracy 4% LSB=5.2V/256=20.3mV Max step error 1 LSB	0
22	DAC3_6		2^6			0
21	DAC3_5		2^5			0
20	DAC3_4		2^4			0
19	DAC3_3		2^3			0
18	DAC3_2		2^2			0
17	DAC3_1		2^1			0
16	DAC3_0		2^0			0
15	DAC2_7		2^7	DAC 2	DAC output voltage: DAC register DAC2=sum(DAC2_i+2^i) VDAC2=5.2V*(DAC2+1)/256 accuracy 4% LSB=5.2V/256=20.3mV Max step error 1 LSB	0
14	DAC2_6		2^6			0
13	DAC2_5		2^5			0
12	DAC2_4		2^4			0
11	DAC2_3		2^3			0
10	DAC2_2		2^2			0
9	DAC2_1		2^1			0
8	DAC2_0		2^0			0
7	DAC1_7		2^7	DAC 1	DAC output voltage: DAC register DAC1=sum(DAC1_i+2^i) VDAC1=5.2V*(DAC1+1)/256 accuracy 4% LSB=5.2V/256=20.3mV Max step error 1 LSB	0
6	DAC1_6		2^6			0
5	DAC1_5		2^5			0
4	DAC1_4		2^4			0
3	DAC1_3		2^3			0
2	DAC1_2		2^2			0
1	DAC1_1		2^1			0
0	DAC1_0		2^0			0

Table 20 Subaddress 06H, Mode Bytes, Test Mode and Standby Control

Bit	Symbol	Bits	V	Function	Description	Defaults
15	CPT	0		Charge pump test mode control	CP is in normal mode (=bipolar)	0
		1			CP current sink or source (=monopolar)	
14	CPP	0			CP = sinking current if CPT=1	0
		1			CP = sourcing current if CPT=1	
13	PT	0		Ports test mode control	Ports in normal mode (=bits P0, P1 to ports)	0
		1			Ports in test mode (=RFAGC Detector or $f_{PD/2}$)	
12	PTSEL	0		Ports test output select	RFAGC_WB, RFAGC_NB to P0, P1 if PT=1	0
		1			$f_{PD/2}$ to P0, P1 if PT=1[1)]	
11	STBY11	1		Standby for:	DAC over $V_{prot.}$ disable	0
10	STBY10	1		Standby for:	DAC	1
9	STBY9	1		Standby for:	Integrator	1
8	STBY8	1		Standby for:	IFAGC	1
7	STBY7	1		Standby for:	SAW driver	1
6	STBY6	1		Standby for:	Mixer + RFAGC	1
5	STBY5	1		Standby for:	Ports	1
4	STBY4	1		Standby for:	PLL (and Rfosc/3)	1
3	STBY3	1		Standby for:	RF oscillator	1
2	STBY2	1		Standby for:	DCDC converter	1

Bit	Symbol	Bits	V	Function	Description	Defaults
1	STBY1	1		Standby for:	Crystal oscillator	0
0	STBY0	1		Standby for:	BIAS (disables all except bus)	0

1) P0, P1 are outputs for f_{ref}, f_{div}.
P0 is output for f_{ref} divided by 2. P1 is output for f_{div} divided by 2.

5.5.2 Read Data Registers

Table 21 Subaddress 80H, Status

Bit	Symbol	Bits	V	Function	Description
7	POF			Power-on flag	=1 after power-on. Reset after first read of register
6	LF			Lock-in flag	=1 if lock-in
5				not used	
4	RFAGC			RFAGC flag	=1 if RFAGC is active (< 3V)
3	RFAGC_NB			NB detector flag	=1 if NB detector is above threshold =0 if NB detector is below threshold
2	RFAGC_WB			WB detector flag	=1 if WB detector is above threshold =0 if WB detector is below threshold
1	P1			Port P1 input	=1 if P1 is high
0	P0			Port P0 input	=1 if P0 is high

Table 22 Subaddress 8EH, Chip Code “6041”

Bit	Symbol	Bits	V	Function	Description	Defaults
15	CC15		2^{15}	Chip Code (binary coded)	$CC = 2^{15} \times CC15 + 2^{14} \times CC14 + ... + 2^{1} \times CC1 + 2^{0} \times CC0$	0
14	CC14		2^{14}			0
13	CC13		2^{13}			0
12	CC12		2^{12}			1
11	CC11		2^{11}			0
10	CC10		2^{10}			1
9	CC9		2^{9}			1
8	CC8		2^{8}			1
7	CC7		2^{7}			1
6	CC6		2^{6}			0
5	CC5		2^{5}			0
4	CC4		2^{4}			1
3	CC3		2^{3}			1
2	CC2		2^{2}			0
1	CC1		2^{1}			0
0	CC0		2^{0}			1

Table 23 **Subaddress 8FH,** Revision Code, advanced with design steps

Bit	Symbol	Bits	V	Function	Description	Defaults
15	RC15			Revision Code (ASCII coded)	first digit	depends on design step
14	RC14					
13	RC13					
12	RC12					
11	RC11					
10	RC10					
9	RC9					
8	RC8					
7	RC7				second digit	
6	RC6					
5	RC5					
4	RC4					
3	RC3					
2	RC2					
1	RC1					
0	RC0					

5.6 Measurement Circuits

5.6.1 Gain (G_V) measurement in LOW band

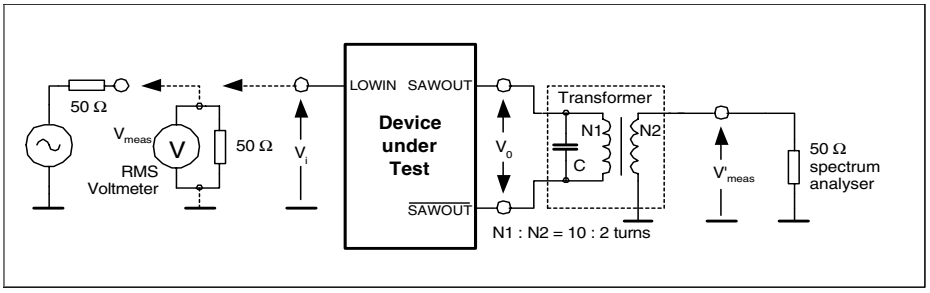


Figure 9 Gain (G_V) measurement in LOW band

- Z_i >> 50 Ω => V_i = 2 x V_{meas} = 80 dBµV
- V_i = V_{meas} + 6dB = 80 dBµV
- V_0 = V'_{meas} + 17 dB (transformer ratio N1:N2 and transformer loss)
- G_v = 20 log(V_0 / V_i)

5.6.2 Gain (G_V) measurement in MID and HIGH bands

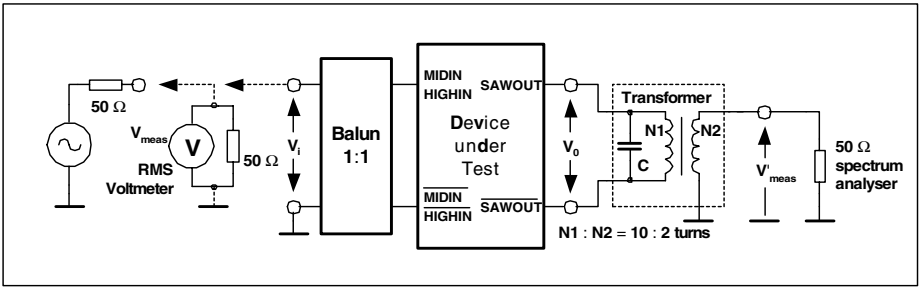
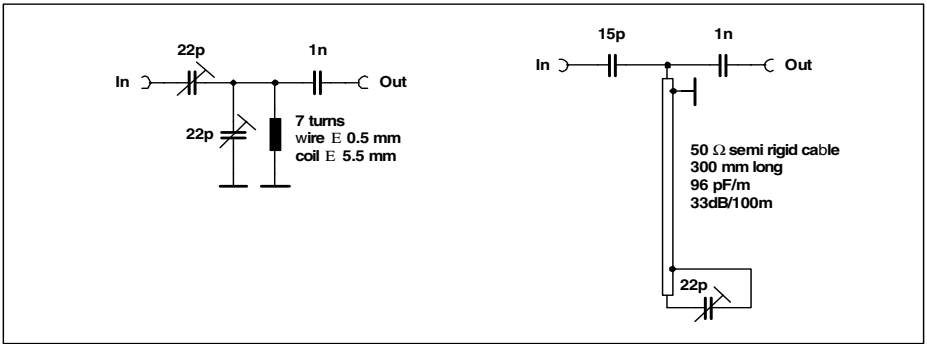


Figure 10 Gain (G_V) measurement in MID and HIGH bands

- V_i = V_{meas} = 70 dBµV
- V_0 = V'_{meas} + 17 dB (transformer ratio N1:N2 and transformer loss
- G_v = 20 log(V_0 / V_i) + 1 dB (1 dB = insertion loss of balun)

5.6.3 Matching circuit for optimum noise figure in LOW band



For f_{RF} = 50 MHz
loss = 0 dB
image suppression = 16 dB

For f_{RF} = 150 MHz
loss = 1.3 dB
image suppression = 13 dB

Figure 11 Matching circuit for optimum noise figure in LOW band

5.6.4 Noise figure (NF) measurement in LOW band

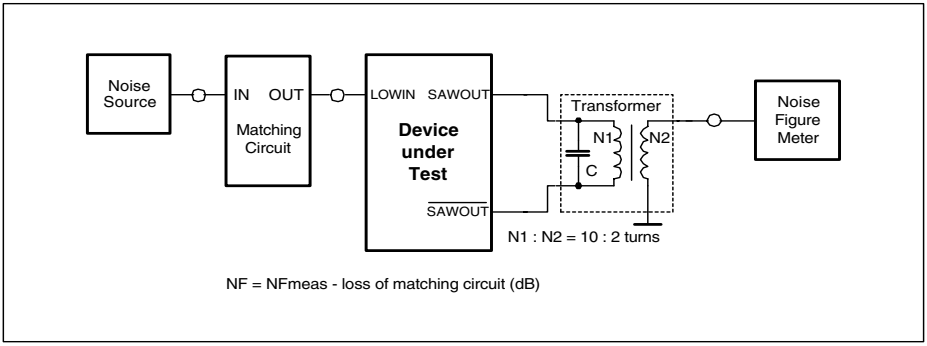


Figure 12 Noise figure (NF) measurement in LOW band

5.6.5 Noise figure (NF) measurement in MID and HIGH bands

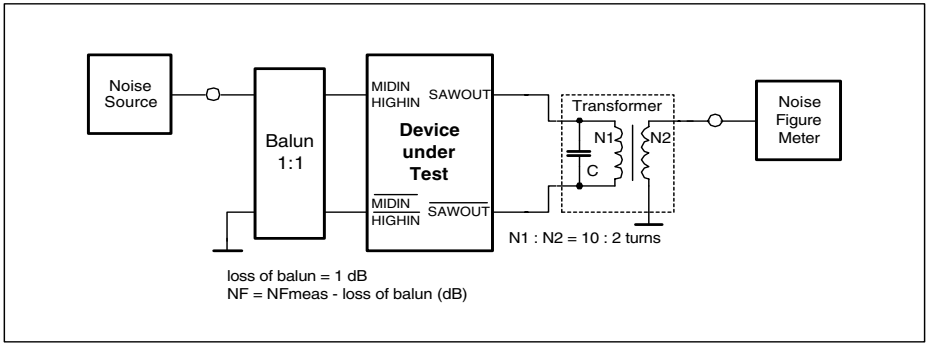


Figure 13 Noise figure (NF) measurement in MID and HIGH bands

5.6.6 Cross modulation measurement in LOW band

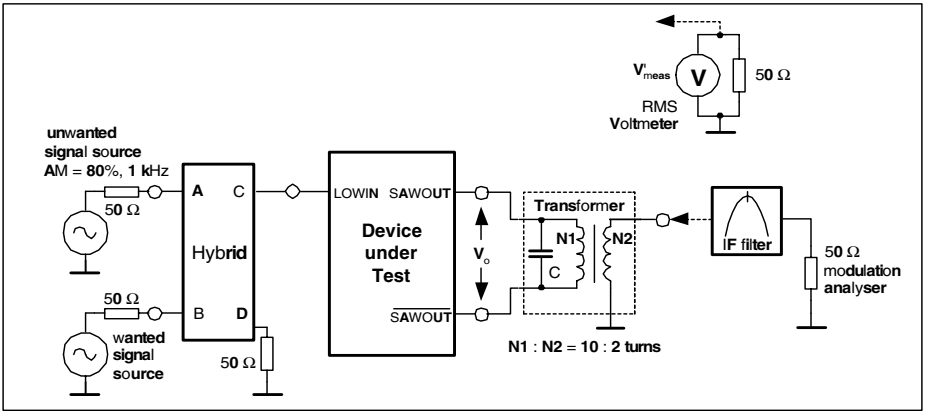


Figure 14 Cross modulation measurement in LOW band

- $V'_{meas} = V_o$ - 17 dB (transformer ratio N1:N2 and transformer loss)
- wanted output signal at f_{pix}, V_o = 100 dBµV
- unwanted output signal at f_{snd}

5.6.7 Cross modulation measurement in MID and HIGH bands

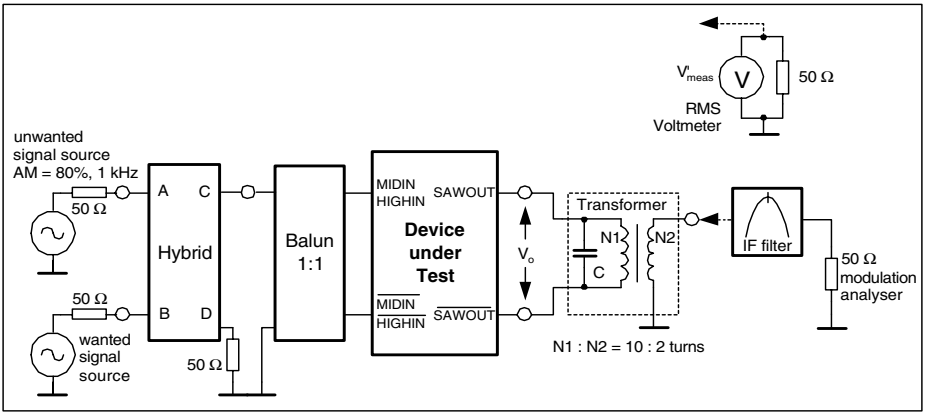


Figure 15 Cross modulation measurement in MID and HIGH bands

- $V'_{meas} = V_o$ - 17 dB (transformer ratio N1:N2 and transformer loss)
- wanted output signal at f_{pix}, V_o = 100 dBµV
- unwanted output signal at f_{snd}

5.6.8 Ripple susceptibility measurement

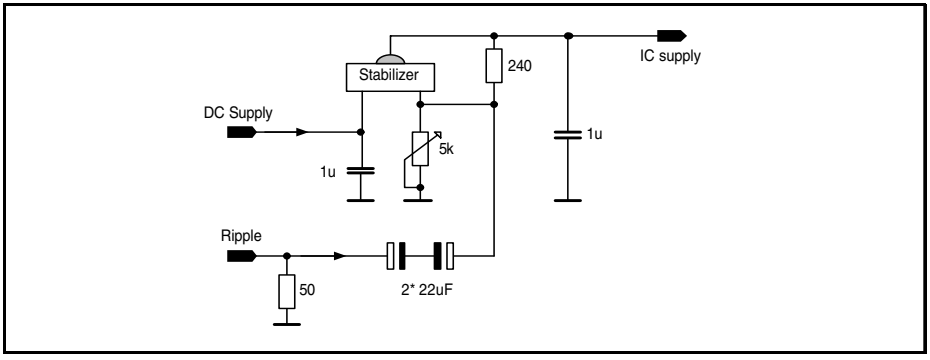


Figure 16 Ripple susceptibility measurement

6 Package PG-VQFN-48

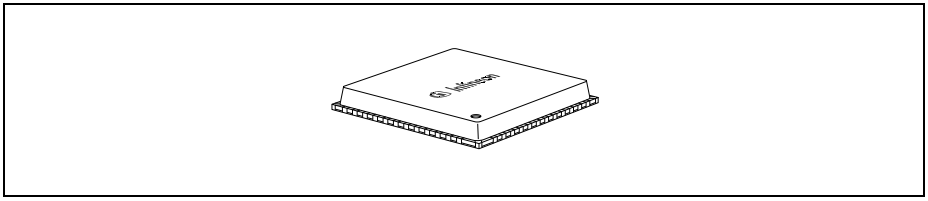


Figure 17 PG-VQFN-48 Vignette

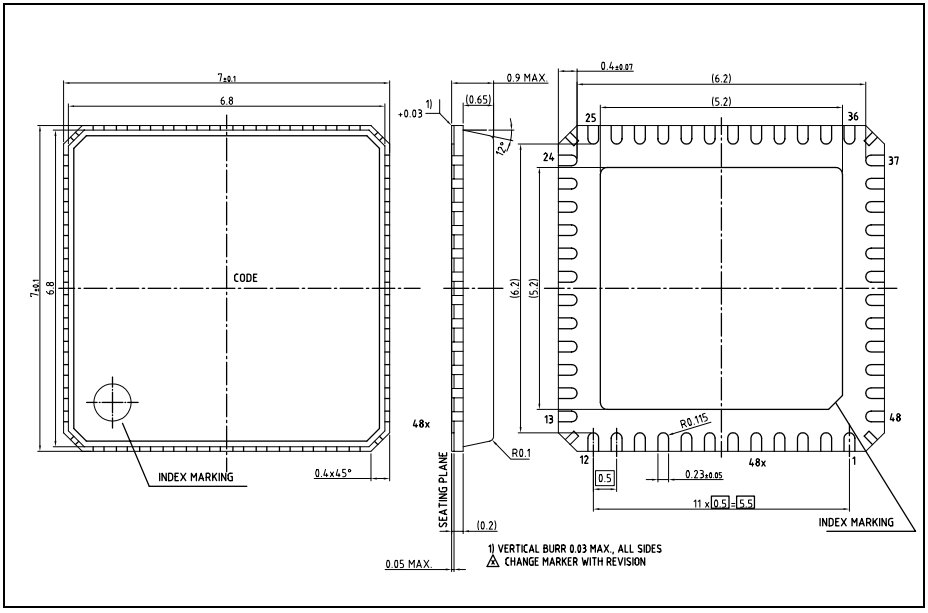


Figure 18 PG-VQFN-48 Outline Drawing

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

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