ON Semiconductor

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NTD50N03R

Power MOSFET

25 V, 45 A, Single N−Channel, DPAK

Features

- Planar Technology
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Pb−Free Packages are Available

Applications

- VCORE DC−DC Buck Converter Applications
- Optimized for High Side Switching

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	25	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current ($R_{\theta JA}$) (Note 1)	Steady State	T_A = 25°C	I_D	9.2	A
		T_A = 85°C		7.2	
Power Dissipation ($R_{\theta JA}$) (Note 1)		T_A = 25°C	P_D	2.1	W
Continuous Drain Current ($R_{\theta JA}$) (Note 2)		T_A = 25°C	I_D	7.8	A
		T_A = 85°C		6.0	
Power Dissipation ($R_{\theta JA}$) (Note 2)		T_A = 25°C	P_D	1.5	W
Continuous Drain Current ($R_{\theta JC}$) (Note 1)		T_C = 25°C	I_D	45	A
		T_C = 85°C		35	
Power Dissipation ($R_{\theta JC}$) (Note 1)		T_C = 25°C	P_D	50	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	180	A
Current Limited by Package	T_A = 25°C		$I_{DmaxPkg}$	45	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 175	°C
Source Current (Body Diode)			I_S	45	A
Drain−to−Source (dv/dt)			dv/dt	8.0	V/ns
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, V_{DD} = 50 V, V_{GS} = 10 V, I_L = 6.32 A_{pk}, L = 1.0 mH, R_G = 25 Ω)			E_{AS}	20	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface−mounted on FR4 board using 1 sq in pad, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size.

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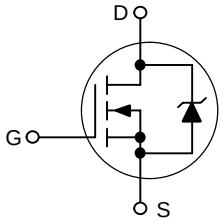
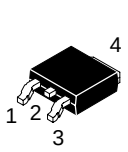
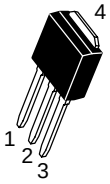
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
25 V	12.5 mΩ @ 10 V	45 A
	19 mΩ @ 4.5 V	

N−Channel

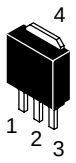




CASE 369AA
DPAK
(Surface Mount)
STYLE 2

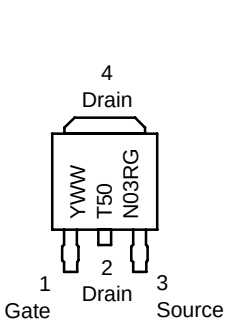


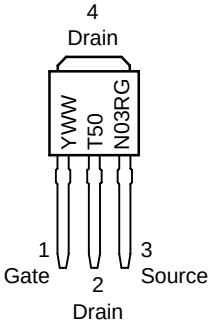
CASE 369D
DPAK
(Straight Lead)
STYLE 2



CASE 369AC
3 IPAK
(Straight Lead)

MARKING DIAGRAMS & PIN ASSIGNMENTS





Y	= Year
WW	= Work Week
T50N03R	= Device Code
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Drain)	$R_{\theta JC}$	3.0	°C/W
Junction−to−Ambient − Steady State (Note 3)	$R_{\theta JA}$	71.4	
Junction−to−Ambient − Steady State (Note 4)	$R_{\theta JA}$	100	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		25			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				−16		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 20 V	T_J = 25°C			1.5	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.0	1.7	2.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−5.0		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 11.5 V	I_D = 30 A		12		mΩ
			I_D = 15 A		11.7		
		V_{GS} = 10 V	I_D = 30 A		12.5	14	
		V_{GS} = 4.5 V	I_D = 30 A		21		
			I_D = 15 A		19	23	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 15 A			15		S
CHARGES, CAPACITANCES AND GATE RESISTANCE							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 12 V			610	750	pF
Output Capacitance	C_{oss}				300		
Reverse Transfer Capacitance	C_{rss}				125		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 30 A			6.0	10	nC
Threshold Gate Charge	$Q_{G(TH)}$				0.9		
Gate−to−Source Charge	Q_{GS}				1.9		
Gate−to−Drain Charge	Q_{GD}				3.7		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 11.5 V, V_{DS} = 15 V, I_D = 30 A			15		nC
Threshold Gate Charge	$Q_{G(TH)}$				1.0		
Gate−to−Source Charge	Q_{GS}				1.9		
Gate−to−Drain Charge	Q_{GD}				3.9		

3. Surface−mounted on FR4 board using 1 sq in pad, 1 oz Cu.
4. Surface−mounted on FR4 board using the minimum recommended pad size.
5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS (continued) (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 6)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 30 A, R_G = 3.0 Ω			8.2		ns
Rise Time	t_r				9.6		
Turn−Off Delay Time	$t_{d(off)}$				11.2		
Fall Time	t_f				6.8		
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 11.5 V, V_{DS} = 15 V, I_D = 30 A, R_G = 3.0 Ω			5.0		ns
Rise Time	t_r				84		
Turn−Off Delay Time	$t_{d(off)}$				15		
Fall Time	t_f				4.0		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 30 A	T_J = 25°C		0.85	1.1	V
			T_J = 125°C		0.71		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 30 A			24		ns
Charge Time	t_a				14		
Discharge Time	t_b				10.5		
Reverse Recovery Charge	Q_{RR}				14		nC
PACKAGE PARASITIC VALUES							
Source Inductance	L_S	Ta = 25C			2.49		nH
Drain Inductance	L_D				0.02		
Gate Inductance	L_G				3.46		
Gate Resistance	R_G				3.75		Ω

6. Switching characteristics are independent of operating junction temperatures.

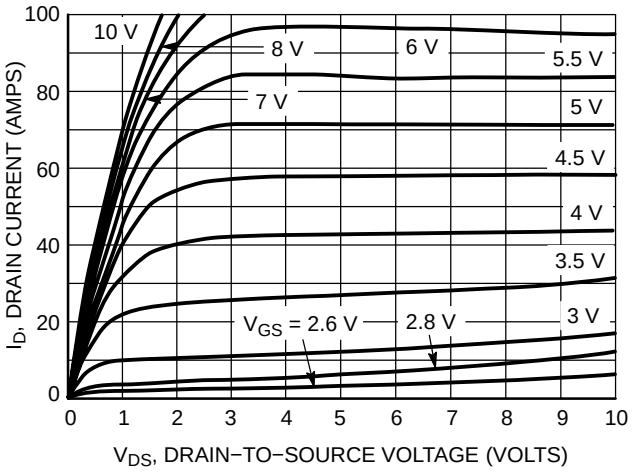


Figure 1. On−Region Characteristics

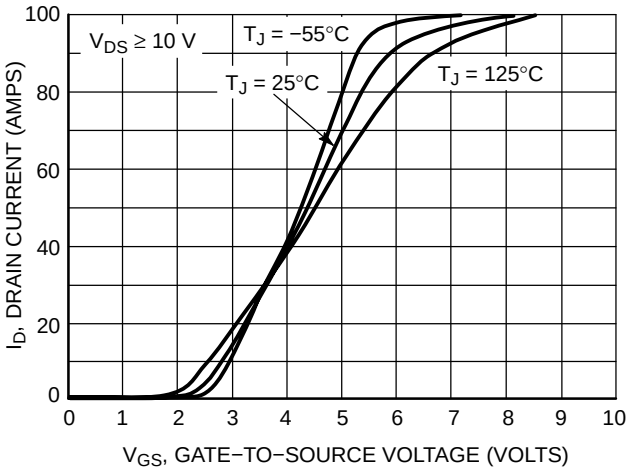


Figure 2. Transfer Characteristics

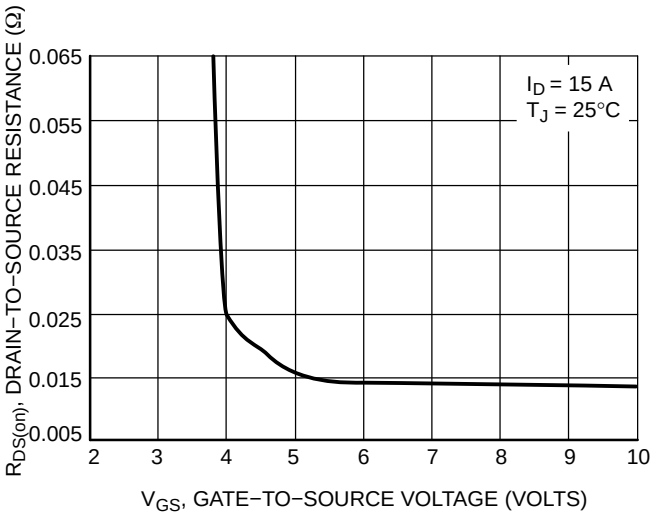


Figure 3. On−Resistance versus Gate−to−Source Voltage

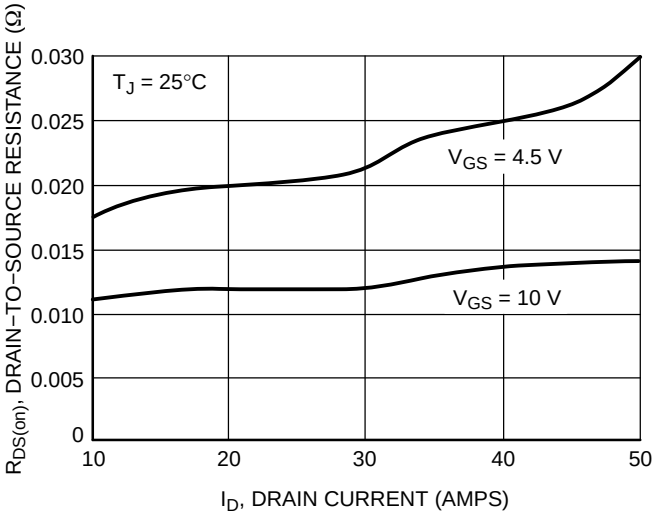


Figure 4. On−Resistance versus Drain Current and Gate Voltage

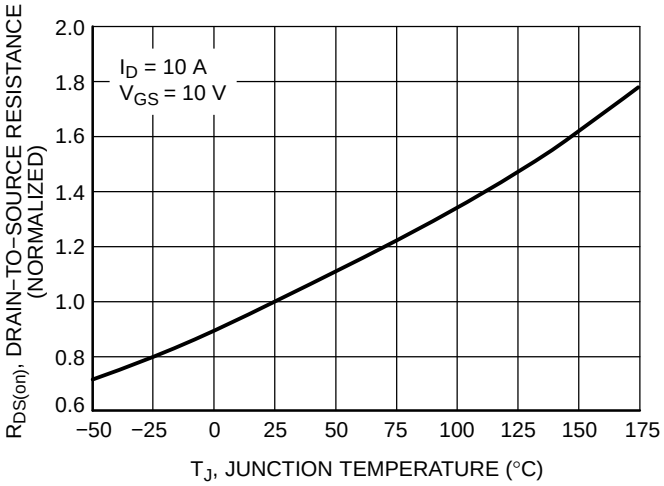


Figure 5. On−Resistance Variation with Temperature

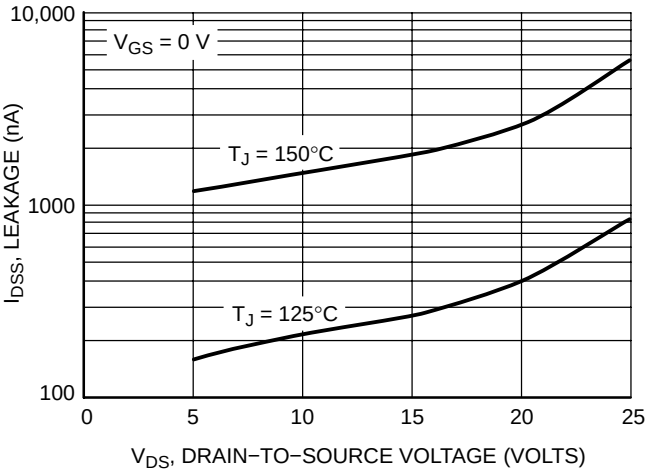


Figure 6. Drain−to−Source Leakage Current versus Voltage

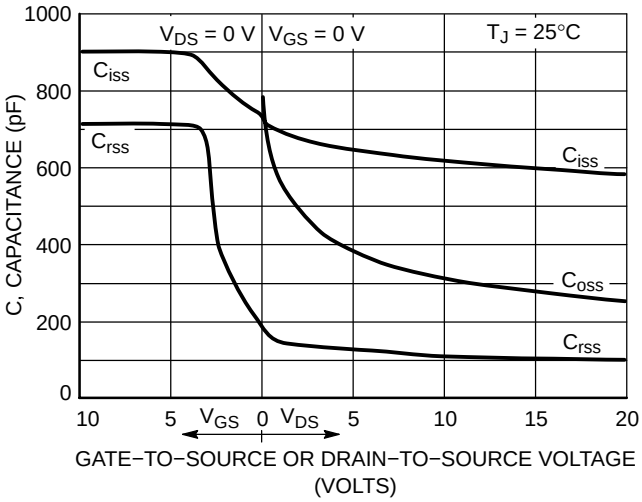


Figure 7. Capacitance Variation

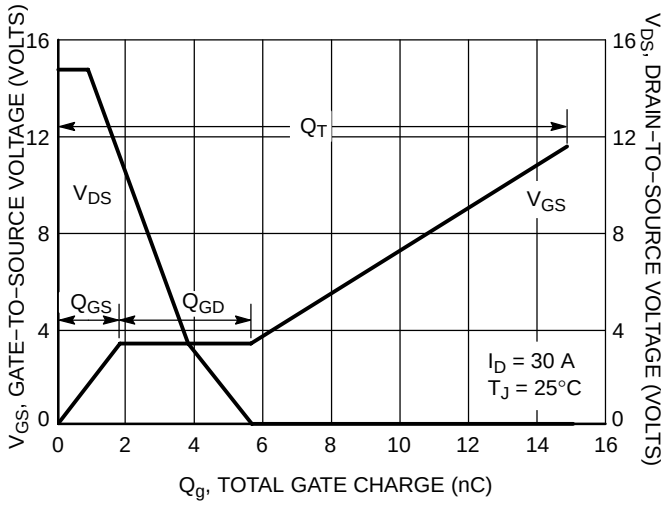


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

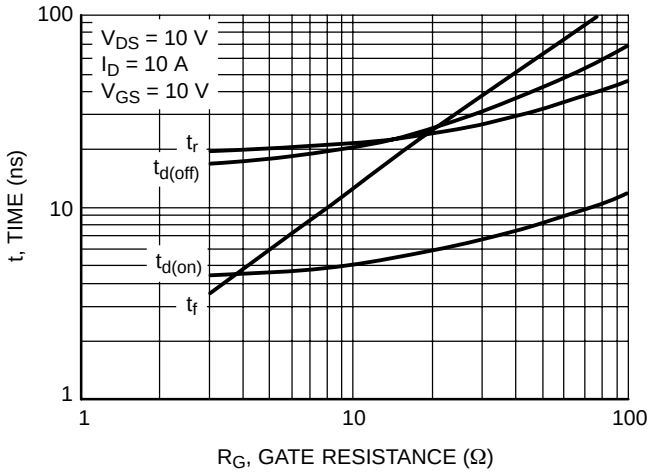


Figure 9. Resistive Switching Time Variation versus Gate Resistance

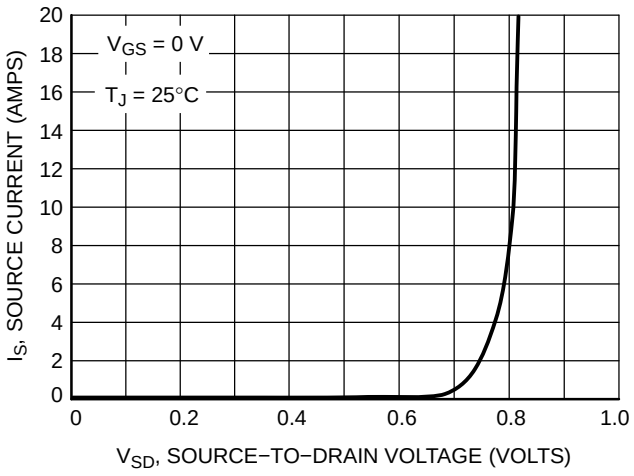


Figure 10. Diode Forward Voltage versus Current

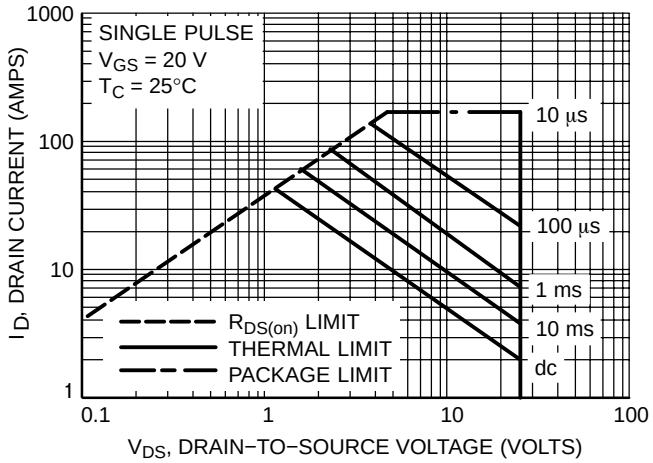


Figure 11. Maximum Rated Forward Biased Safe Operating Area

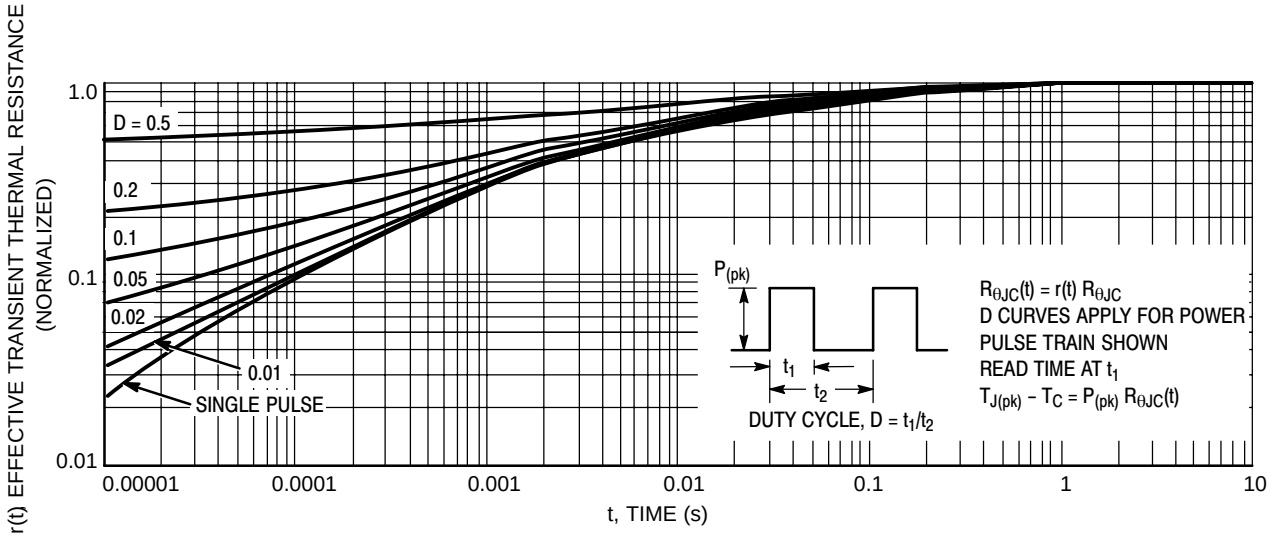


Figure 12. Thermal Response

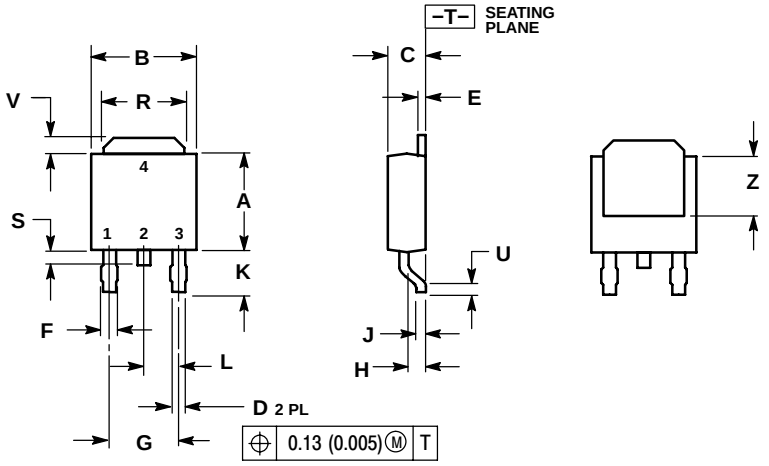
ORDERING INFORMATION

Order Number	Package	Shipping†
NTD50N03R	DPAK−3	75 Units / Rail
NTD50N03RG	DPAK−3 (Pb−Free)	75 Units / Rail
NTD50N03RT4	DPAK−3	2500 / Tape & Reel
NTD50N03RT4G	DPAK−3 (Pb−Free)	2500 / Tape & Reel
NTD50N03R−1	DPAK−3 Straight Lead	75 Units / Rail
NTD50N03R−1G	DPAK−3 Straight Lead (Pb−Free)	75 Units / Rail
NTD50N03R−35	DPAK−3 Straight Lead Trimmed (3.5 ± 0.15 mm)	75 Units / Rail
NTD50N03R−35G	DPAK−3 Straight Lead Trimmed (3.5 ± 0.15 mm) (Pb−Free)	75 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

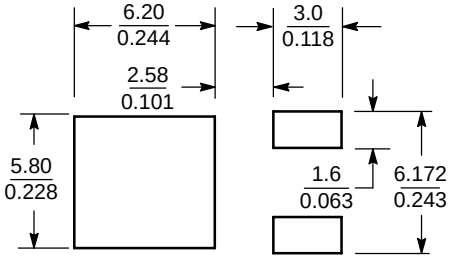
DPAK
CASE 369C−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

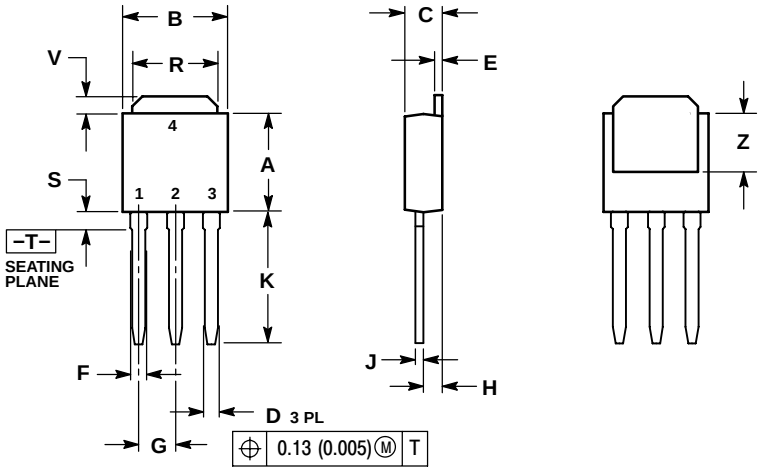
SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DPAK
CASE 369D−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
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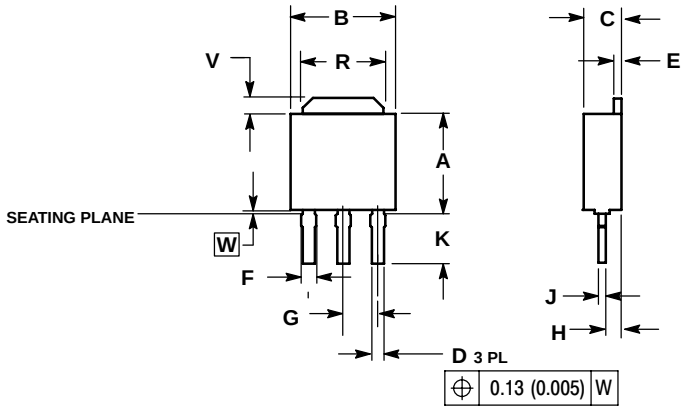
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PACKAGE DIMENSIONS

3 IPAK, STRAIGHT LEAD
CASE 369AC−01
ISSUE O



NOTES:
1.. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2.. CONTROLLING DIMENSION: INCH.
3. SEATING PLANE IS ON TOP OF DAMBAR POSITION.
4. DIMENSION A DOES NOT INCLUDE DAMBAR POSITION OR MOLD GATE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.043	0.94	1.09
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.134	0.142	3.40	3.60
R	0.180	0.215	4.57	5.46
V	0.035	0.050	0.89	1.27
W	0.000	0.010	0.000	0.25

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

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NTD50N03R/D