UCC28250 Advanced PWM Controller With Prebias Operation

1 Features

- Prebiased Start-up
- Synchronous Rectifier Control Outputs With Programmable Delays (Including Zero Delay Support)
- Voltage Mode Control With Input Voltage Feed-Forward or Current Mode Control
- Primary or Secondary-Side Control
- 3.3-V, 1.5% Accurate Reference Output
- 1-MHz Capable Switching Frequency
- 1% Accurate Cycle-by-Cycle Overcurrent Protection with Matched Duty Cycle Outputs
- Programmable Soft-Start and Hiccup Restart Timer
- Thermally Enhanced 4-mm × 4-mm QFN-20 Package and 20-pin TSSOP Package

2 Applications

- Half-Bridge, Full-Bridge, Interleaved Forward, and Push-Pull Isolated Converters
- Telecom and Data-com Power
- Wireless Base Station Power
- Server Power
- Industrial Power Systems

3 Description

The UCC28250 PWM controller is designed for high power density applications that may have stringent prebiased start-up requirements. The integrated synchronous rectifier control outputs target high-efficiency and high-performance topologies such as half-bridge, full-bridge, interleaved forward, and push-pull. The UCC27200 half-bridge drivers and UCC2732X MOSFET drivers used in conjunction with the UCC28250 provide a complete power converter solution.

Externally programmable soft-start, used in conjunction with an internal prebiased start-up circuit, allows the controller to gradually reach a steady-state operating point under all output conditions. The UCC28250 can be configured for primary or secondary-side control and either voltage or current mode control can be implemented.

The oscillator operates at frequencies up to 2 MHz, and can be synchronized to an external clock. Input voltage feedforward, cycle-by-cycle current limit, and a programmable hiccup timer allow the system to stay within a safe operation range. Input voltage, output voltage and temperature protection can be implemented. Dead time between primary-side switch and secondary-side synchronous rectifiers can be independently programmed.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC28250	TSSOP (20)	6.50 mm × 4.40 mm
	VQFN (20)	4.00 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram

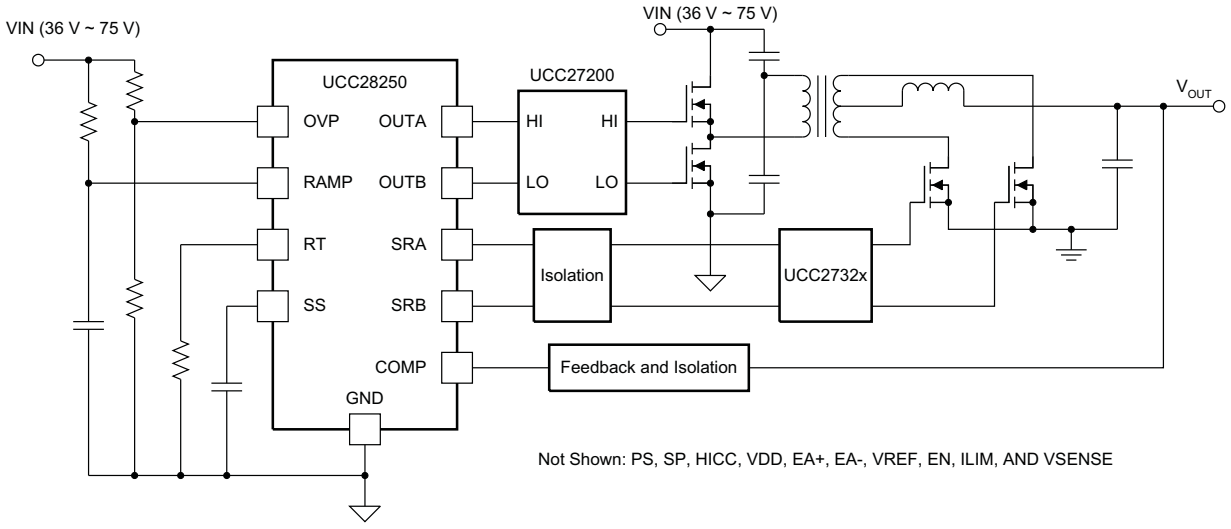


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2011) to Revision D — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision B (October 2010) to Revision C — **Page**

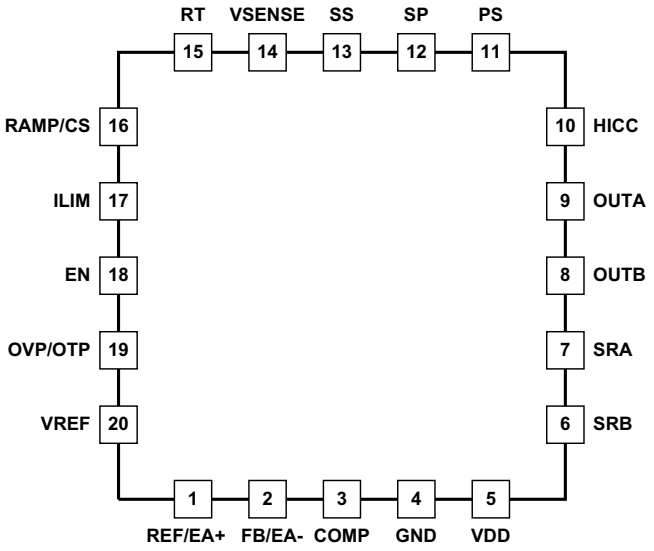
- Changed Operating junction temperature range from (-40 to 125) to (125 to 150). ... 4
- Changed Functional Block Diagram ... 12

Changes from Revision A (April, 2010) to Revision B — **Page**

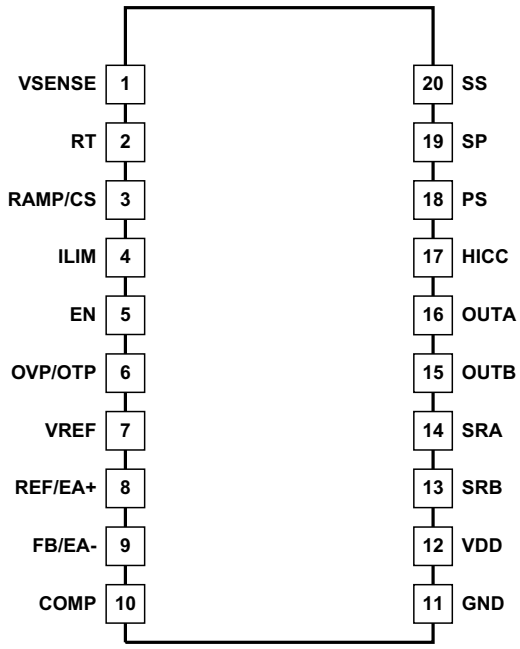
- Added note, "The minimum value for R_{PS}/R_{SP} is 5 kΩ and the maximum value is 250 kΩ." in two places. ... 17

5 Pin Configuration and Functions

RGB Package
20-Pin VQFN
Top View



PW Package
20-Pin TSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	QFN	PW		
COMP	3	10	I/O	Error amplifier output
EN	18	5	I	Device enable and disable
FB/EA-	2	9	I	Error amplifier inverting input
GND	4	11	I	Ground
HICC	10	17	I	Cycle-by-cycle current limit time delay and Hiccup time setting
ILIM	17	4	I	Current sense for cycle-by-cycle overcurrent protection
OUTA	9	16	O	0.2-A sink/source primary switching output
OUTB	8	15	O	0.2-A sink/source primary switching output
OVP/OTP	19	6	I	Overvoltage and overtemperature protection pin
PS	11	18	I	Primary off to synchronous rectifier on dead-time set
RAMP/CS	16	3	I	PWM ramp input (for voltage mode control) or current sense input (for current mode control)
REF/EA+	1	8	I	Error amplifier noninverting input
RT	15	2	I	Oscillator frequency set or synchronous clock input
SP	12	19	I	Synchronous rectifier off to primary on dead-time set
SRA	7	14	O	0.2-A sink/source synchronous rectifier output
SRB	6	13	O	0.2-A sink/source synchronous rectifier output
SS	13	20	I/O	Soft-start programming
VDD	5	12	I	Bias supply input
VREF	20	7	O	3.3-V reference output
VSENSE	14	1	I	Output voltage sensing for prebias control

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range[1][2] (unless otherwise noted)

		MIN	MAX	UNIT
VDD[3]	Input supply voltage	–0.3	20	V
	OUTA, OUTB, SRA and SRB	–0.3	VDD + 0.3	V
	COMP	–0.3	VREF + 0.3	V
	Input voltages on SS and EN	–0.3	5.5	V
	Input voltages on RT, PS, SP, ILIM, OVP, HICC, VSENSE, EA+ and EA-	–0.3	3.6	V
	Input voltage on RAMP/CS	–0.3	4.3	V
	Output voltage on VREF	–0.3	3.6	V
	Lead temperature (soldering 10 sec) PW package	300		°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.
(3) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See *Mechanical, Packaging, and Orderable Information* of the data sheet for thermal limitations and considerations of packages.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.7	12	17	V
Supply bypass capacitor, C_{VDD}	1			µF
VREF bypass capacitor	0.5		2	µF
Error amplifier input common-mode (REF/EA+, FB/EA-)	0		3	V
VSENSE input voltage	0		3.3	V
RT resistor	12.5		200	kΩ
PS, SP resistor	5		250	kΩ
RAMP/CS voltage	0		2.7	V
Operating junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC		UCC28250		UNIT
		RGB (VQFN)	PW (TSSOP)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126 with hot spot, 104 without hot spot	60.3 with hot spot, 39.3 without hot spot	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance		31.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		55.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	0.8		°C/W

6.5 Electrical Characteristics

VDD = 12 V, 1-µF capacitor from VDD and VREF to GND, $T_A = T_J$ = –40°C to 125°C, RT = 75 kΩ connected to ground to set F_{SW} = 200 kHz (unless otherwise noted). (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
$I_{DD(off)}$	Start-up current	VDD = 3.6 V		150	275	µA
I_{DD}	Operating supply current	100-pF capacitor on OUTA, OUTB, SRA and SRB	2	2.7	3.4	mA
$I_{DD(dis)}$	Standby current	EN = 0 V	250	425	600	µA
UNDERVOLTAGE LOCKOUT						
V_{UVLOR}	Start threshold		4	4.3	4.6	V
V_{UVLOF}	Minimum operating voltage after start		3.8	4.1	4.4	V
	Hysteresis		0.15	0.2	0.25	V
SOFT START						
I_{SS}	Soft-start charge current	V_{SS} = 0 V	25	27	29	µA
$V_{SS(max)}$	Clamp voltage		3.3	3.6	4	V
ENABLE (2)						
	Trigger threshold				2.25	V
	Minimum pulse width for pulse enable		3			µs
ERROR AMPLIFIER						
	High-level COMP voltage		2.8	3		V
	Low-level COMP voltage			0.3	0.4	V
	Input offset		-12		12	mV
	Open loop gain		70	100		dB
$I_{COMP(snk)}$	COMP sink current		3	6.5	9	mA
$I_{COMP(src)}$	COMP source current		2	4.5	8	mA
OSCILLATOR						
$F_{SW(nom)}$	Nominal switching frequency at OUTA or OUTB set by RT resistor	RT/SYNC = 75 kΩ, R_{SP} = 20 kΩ	185	200	215	kHz
$F_{SW(min\_sync)}$	Minimum switching frequency at OUTA or OUTB set by external sync frequency	$f_{RT/SYNC}$ = 100 kHz		85		kHz
$F_{SW(max\_sync)}$	Maximum switching frequency at OUTA or OUTB set by external sync frequency	$f_{RT/SYNC}$ = 2.5 MHz		1.15		MHz
	External synchronization signal high		1			V
	External synchronization signal low				0.2	V
VOLTAGE REFERENCE						
V_{VREF}	Output voltage	V_{DD} = from 7 V to 17 V, I_{VREF} = 2 mA	3.22	3.3	3.38	V
		0 < I_{REF} < 10 mA	3.22	3.3	3.38	
	Short circuit current	V_{REF} = 3 V, T_J = 25°C	12	25	40	mA

(1) Typical values for T_A = 25°C.
(2) Refer to EN pin description in .

Electrical Characteristics (continued)

VDD = 12 V, 1-µF capacitor from VDD and VREF to GND, $T_A = T_J$ = –40°C to 125°C, RT = 75 kΩ connected to ground to set F_{SW} = 200 kHz (unless otherwise noted). (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE, CYCLE-BY-CYCLE CURRENT LIMIT WITH HICCUP						
V_{ILIM}	ILIM cycle-by-cycle threshold		0.495	0.502	0.509	V
T_{PDILIM}	Propagation delay from ILIM to OUTA and OUTB outputs	Exclude leading edge blanking	15	25	36	ns
T_{BLANK}	leading edge blanking		40	60	90	ns
	Current limit shutdown delay timing program current	Measured at HICC pin	55	75	95	µA
	Hiccup timing program current	Measured at HICC pin	2	2.7	3.5	µA
V_{HICC_SD}	Current limit shutdown delay timer threshold at HICC		0.55	0.6	0.65	V
V_{HICC_PU}	HICC pullup threshold		2.3	2.4	2.5	V
V_{HICC_RST}	Hiccup restart threshold		0.25	0.3	0.35	V
$V_{CS(max)}$	RAMP/CS clamp voltage	10-V ramp charging voltage source with 40-kΩ current limiting resistor	3.5	4	4.5	V
OVP/OTP COMPARATOR						
V_{OVP}	Internal reference		0.66	0.7	0.74	V
I_{OVP}	Internal current		8.5	11	13.5	µA
PRIMARY OUTPUTS						
	Rise/fall time	C_{LOAD} = 100 pF		8		ns
R_{SRC}	Output source resistance	I_{OUT} = 20 mA	12	20	35	Ω
R_{SNK}	Output sink resistance	I_{OUT} = 20 mA	4	12	30	Ω
SYNCHRONOUS RECTIFIER OUTPUTS						
	Rise/fall time	C_{LOAD} = 100 pF		8		ns
R_{SRC}	Output source resistance	I_{OUT} = 20 mA, VDD = 12 V	12	20	35	Ω
		I_{OUT} = 20 mA, VDD = 5 V	15	25	45	
R_{SNK}	Output sink resistance	I_{OUT} = 20 mA, VDD = 12 V	4	12	30	Ω
TD_{PS}	Primary off to secondary on dead time	PS = VREF	-5	0	7.5	ns
		PS = 27 kΩ	27	40	50	
		PS = 27 kΩ, 25°C	37	40	43	
TD_{SP}	Secondary off to primary on dead time	SP = VREF	-5	0	7.5	ns
		SP = 20 kΩ	30	40	50	
		SP = 20 kΩ, 25°C	37	40	43	

6.6 Typical Characteristics

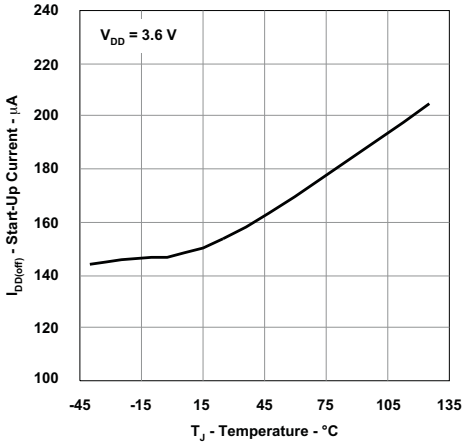


Figure 1. Start-up Current vs Temperature

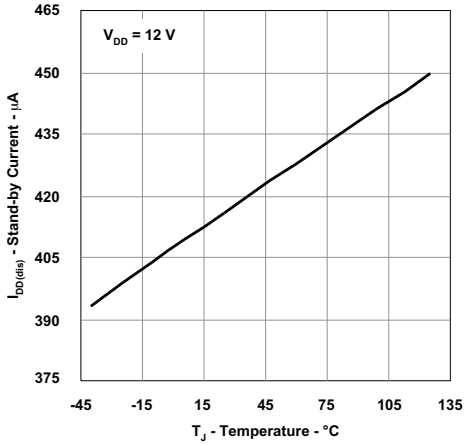


Figure 2. Stand-by Current vs Temperature

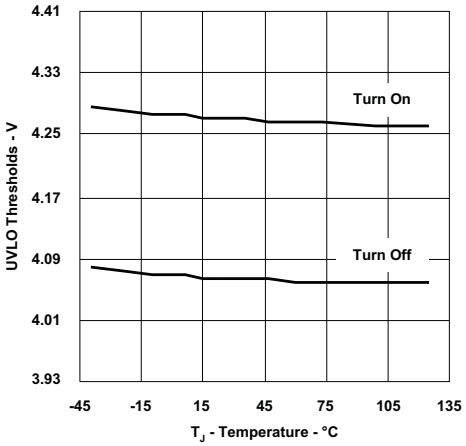


Figure 3. UVLO Thresholds vs Temperature

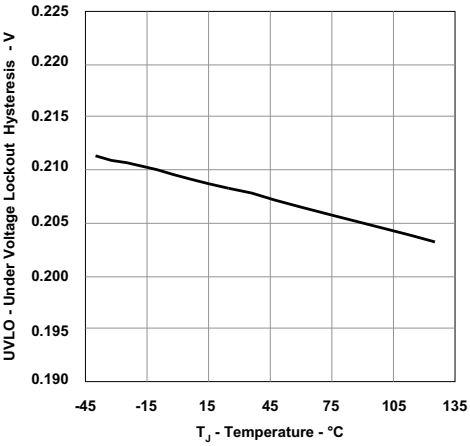


Figure 4. UVLO Voltage Lockout Hysteresis

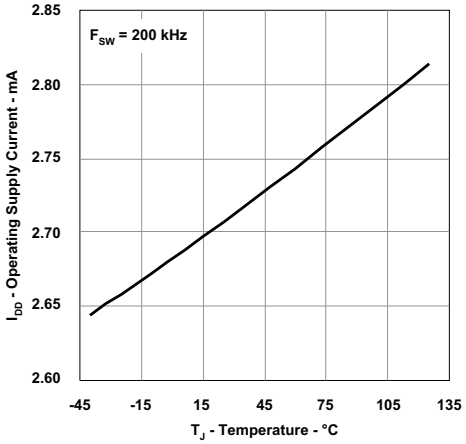


Figure 5. Operating Supply Current vs Temperature

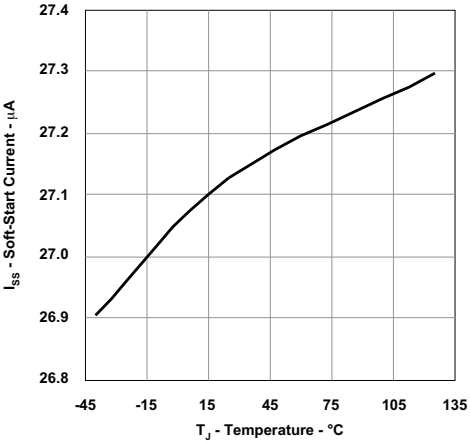


Figure 6. Soft-start Current vs Temperature

Typical Characteristics (continued)

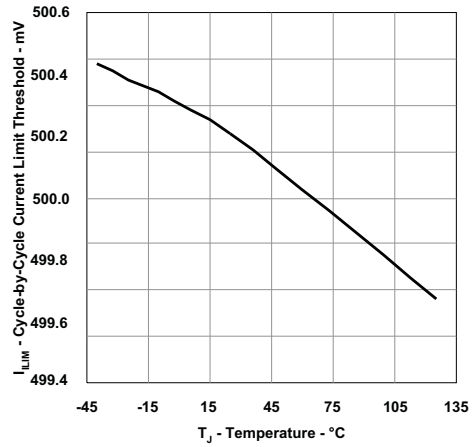


Figure 7. Cycle-by-Cycle Current Limit vs Temperature

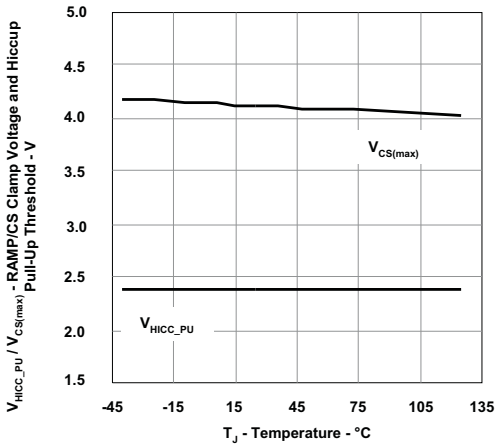


Figure 8. RAMP/CS Clamp Voltage and Hiccup Pullup Threshold vs Temperature

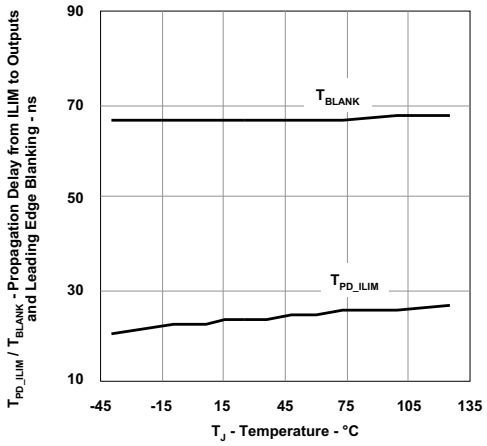


Figure 9. Propagation Delay and Leading Edge Blanking vs Temperature

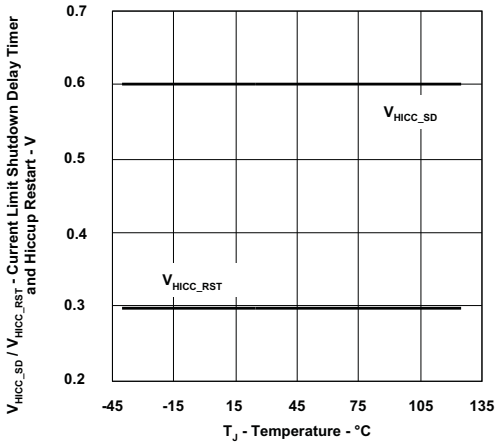


Figure 10. Current Limit Shutdown Delay Timer and Hiccup Restart vs Temperature

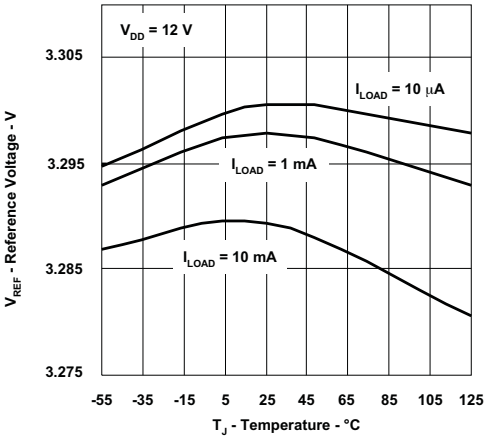


Figure 11. Reference Voltage vs Temperature

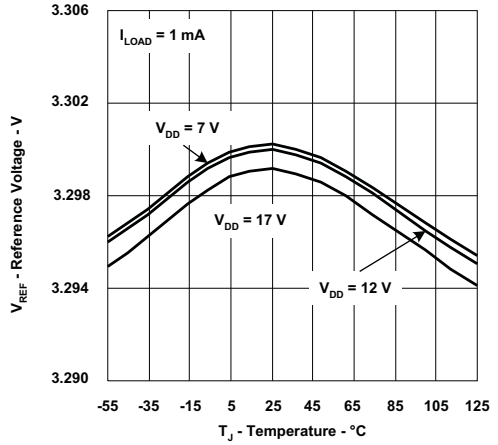


Figure 12. Reference Voltage vs Temperature

Typical Characteristics (continued)

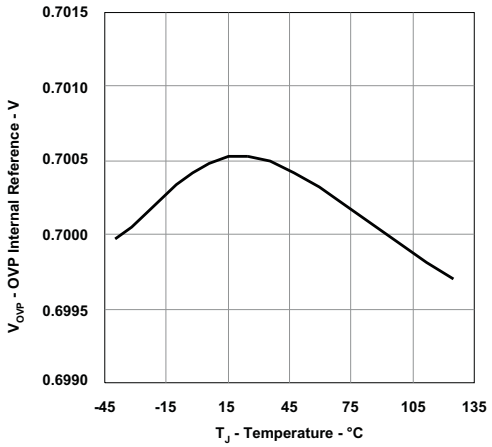


Figure 13. OVP Internal Reference vs Temperature

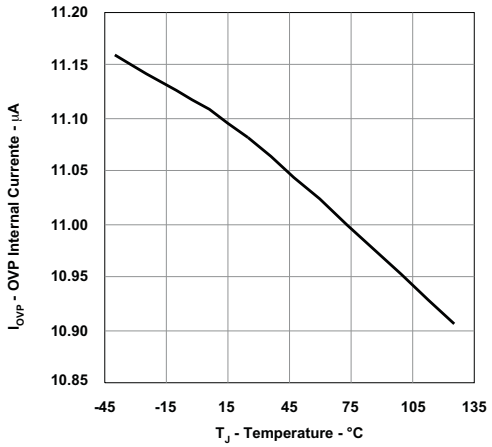


Figure 14. OVP Internal Current vs Temperature

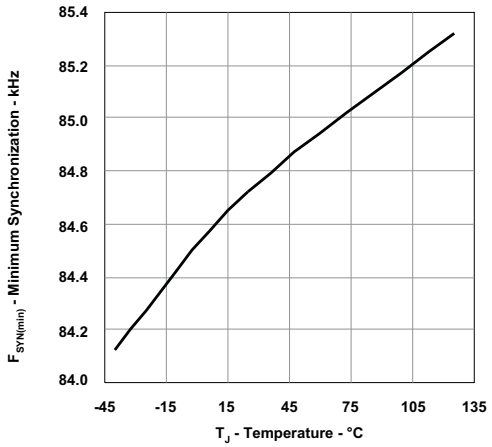


Figure 15. Minimum Synchronization Frequency vs Temperature

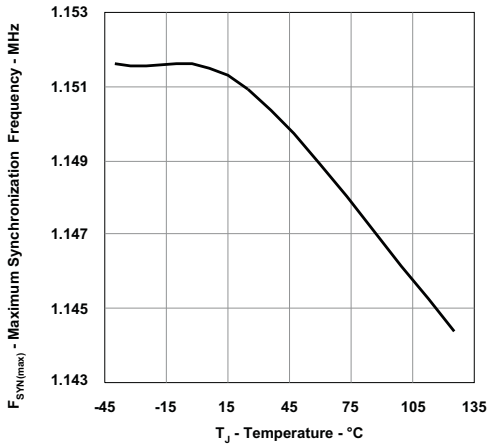


Figure 16. Maximum Synchronization Frequency vs Temperature

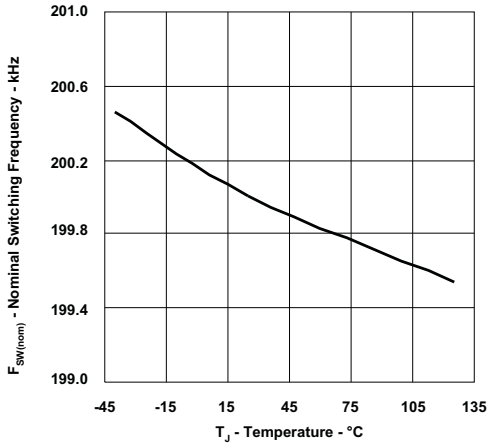


Figure 17. Nominal Switching Frequency vs Temperature

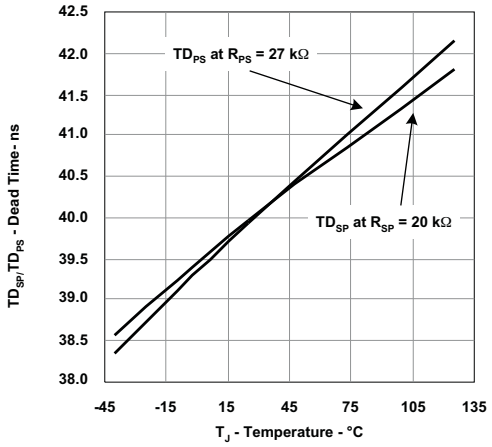


Figure 18. Dead Time vs Temperature

Typical Characteristics (continued)

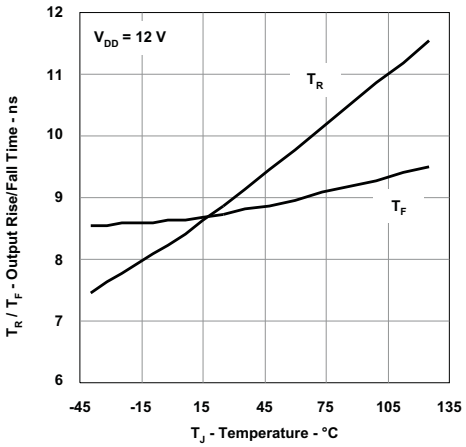


Figure 19. Output Rise/Fall Time vs Temperature

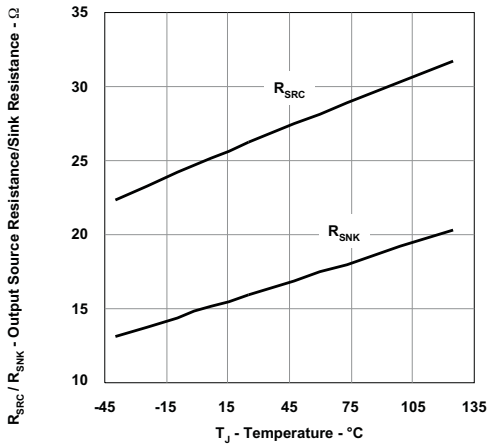


Figure 20. Output Source Resistance/Sink Resistance vs Temperature

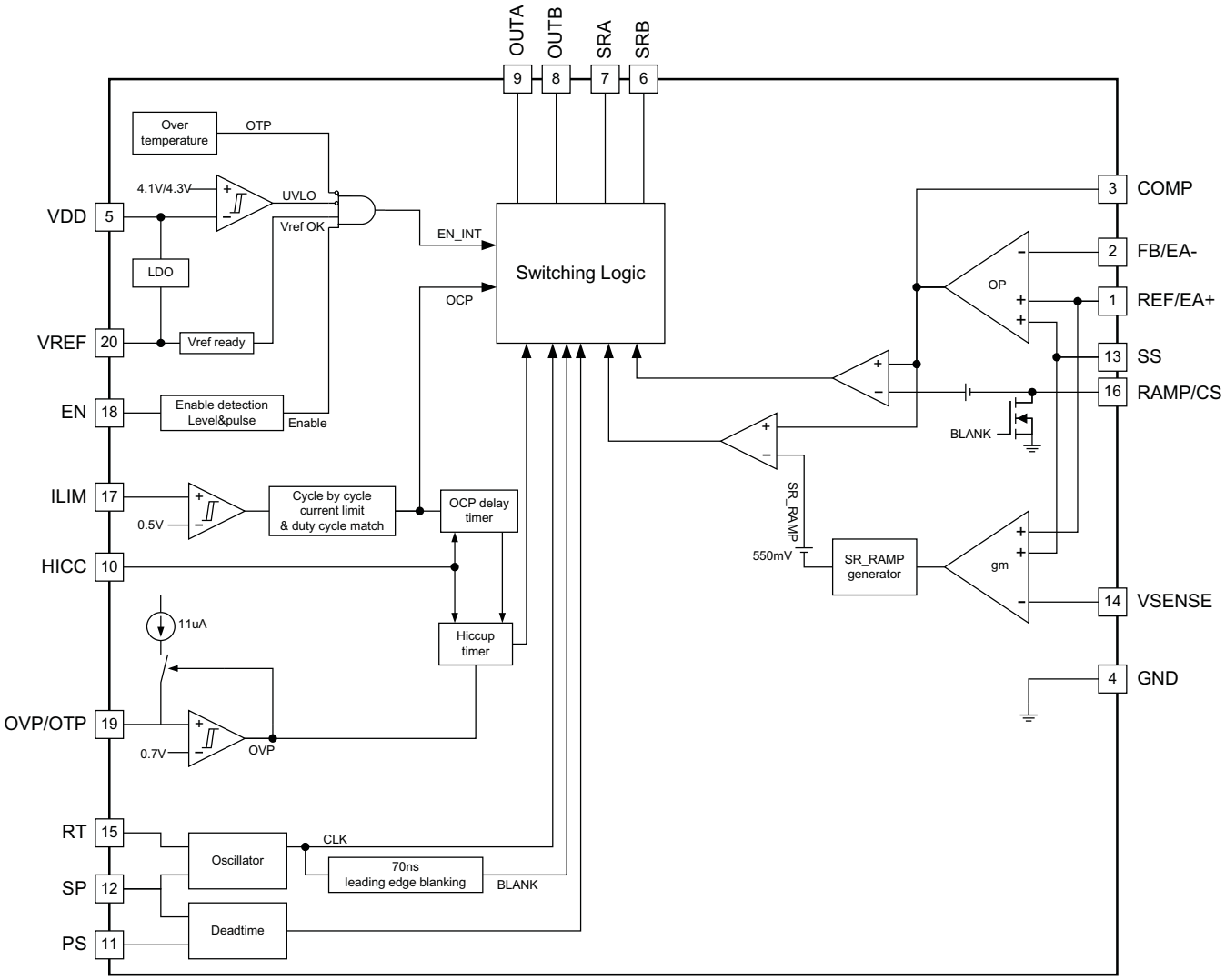
7 Detailed Description

7.1 Overview

The UCC28250 is a high-performance PWM controller with advanced synchronous rectifier outputs and is ideally suited for regulated half-bridge, full-bridge and push-pull converters. A dedicated internal prebiased start-up control loop working in conjunction with a primary-side voltage loop achieves prebiased start-up for either primary-side or secondary-side control applications. The UCC28250 architecture allows either voltage mode or current mode control.

Input voltage feedforward can be implemented, allowing PWM ramp generator to improve the converter line transient response. Advanced cycle-by-cycle current limit achieves volt-second balancing even during fault conditions. The hiccup timer helps the system to stay within a safe operation range under over load conditions. With a multifunction OVP/OTP pin, combinations of input voltage protection, output voltage protection and overtemperature protection can be implemented. The UCC28250 allows individual programming of dead time between primary-side switch and secondary-side SRs, to allow optimal power stage design. Dead time can also be reduced to zero, and this allows optimal system configuration considering the delays on the gate driver stage. The UCC28250 also provides complete system level protection functions, including UVLO, thermal shut down and overvoltage, overcurrent protection.

7.2 Functional Block Diagram



NOTE: Pin numbers are used for RGP package. PW package has different pin numbers.

7.3 Feature Description

7.3.1 VDD (5/12)

The UCC28250 can be powered up by a wide supply range from 4.3 V (UVLO rising typical) to 20 V (absolute maximum), making it suitable for primary-side control or secondary-side control. When the voltage at the VDD pin is lower than 4.1 V (typical), the controller is in stand-by mode and consumes 150 µA (typical) at 3.6 V VDD. In stand-by mode, VREF continues to be regulated to 3.3 V or follows VDD if VDD is lower than 3.3 V. Refer to the VREF description *VREF (Reference Generator) (20/7)* for more detailed information. A minimum 1-µF bypass capacitor is required from VDD to ground. Keep the bypass capacitor as close to the device as possible.

7.3.2 VREF (Reference Generator) (20/7)

The VREF pin is regulated at 3.3 V. An external ceramic capacitor must be placed as close as possible to the VREF and GND pins for noise filtering and to provide compensation to the regulator. The capacitance range must be limited from 0.5 µF to 2 µF for stability. This reference is used to power the controller's internal circuits, and can also be used to bias an opto-coupler transistor, an external house-keeping microcontroller, or other peripheral circuits. This reference can also be used to generate the reference for an external error amplifier. This regulator output is internally current limited to 25 mA (typical).

Feature Description (continued)

7.3.3 EN (Enable Pin) (18/5)

The following conditions must be met before the controller allows start-up:

1. VDD voltage is above the rising UVLO threshold 4.3 V (typical).
2. The 3.3-V reference voltage output at the VREF pin is available and above 2.4 V (typical).
3. Junction temperature is below the thermal shutdown threshold 130°C (minimum).
4. The voltage at OVP is below 0.7 V (typical).

If all these conditions are met, the signal driving the EN pin is able to initiate the soft start process. When the device is enabled, the 27-µA internal charging current at the SS pin is turned on and begins to charge the soft-start capacitor. The EN pin can accept both level-enable and pulse-enable signals.

For level-enable, the voltage level on the EN pin must be continuously higher than 2.25 V to allow continuous operation. When the EN pin falls below 2.25 V, the device is disabled (see Figure 21).

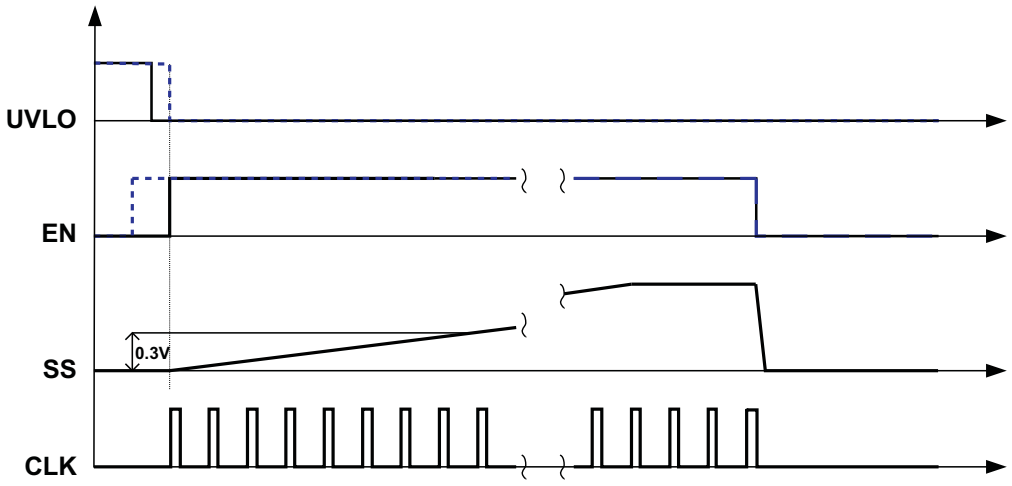


Figure 21. Level Enable at EN pin

Feature Description (continued)

A pulse signal may also be applied to the EN pin. Pulse-enable operation is shown on Figure 22. As long as the EN falling edge happens before the SS voltage reaches 0.3 V, the enable signal at EN pin is considered as a pulse. In this case, the next rising edge at EN pin disables the controller. As long as the falling edge of the first pulse at EN pin happens after SS rises to 0.3 V, the UCC28250 interprets the pulse enable as a level enable, and an external solution as shown on Figure 23 (a) can be used to reduce the pulse width. In this circuit, R2 is used to limit the current (especially the negative current) through the internal ESD cell. Figure 23 (b) illustrates the waveforms based on this solution. To prevent false trigger by noises, the pulse at the EN pin must be at least 2.25 V (minimum) high and 3 µs wide to be considered valid.

Choose the R1, R2, and C values based on the following equations:

Choose R2 based on the current limit requirement from the device.

$$R_2 > 10\,k\Omega \tag{1}$$

Choose R1 arbitrarily but much smaller than R2 and choose C1 according to the time constant requirement to generate longer than 3-µs pulse.

$$C_1 = \frac{6\,\mu s}{R_1} \tag{2}$$

In the case that the UCC28250 is enabled with a level EN signal and the SS is discharged internally when the OCP is triggered, pulling the EN pin down before SS rises to 0.3 V cannot disable the part because the controller interprets it to be a pulse enable. In this case, the next rising edge at the EN pin disables the controller. If the designer wants to disable UCC28250 with a level signal during an over current condition, the recommended solution is to pull down the SS pin rather than the EN pin. If the enable function is not used, pull the EN pin to the VREF pin.

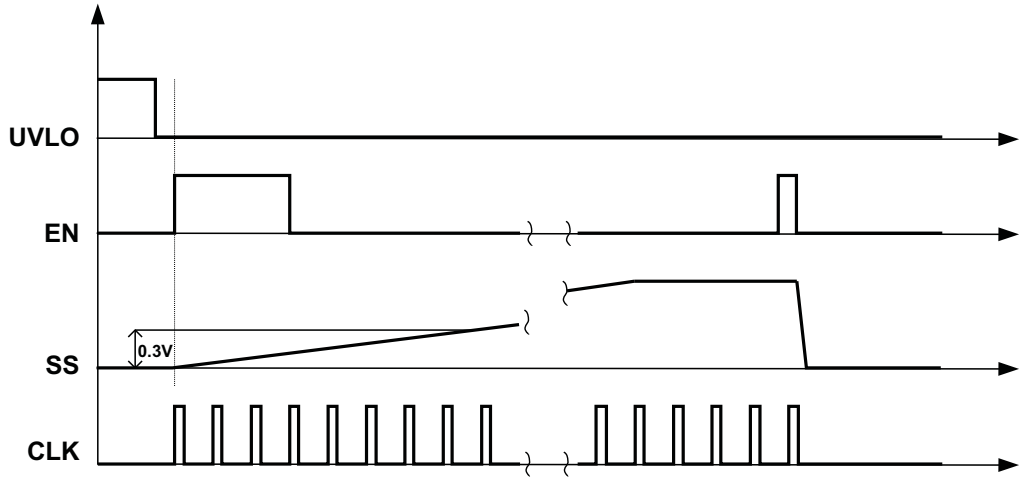


Figure 22. Pulse Enable at EN Pin

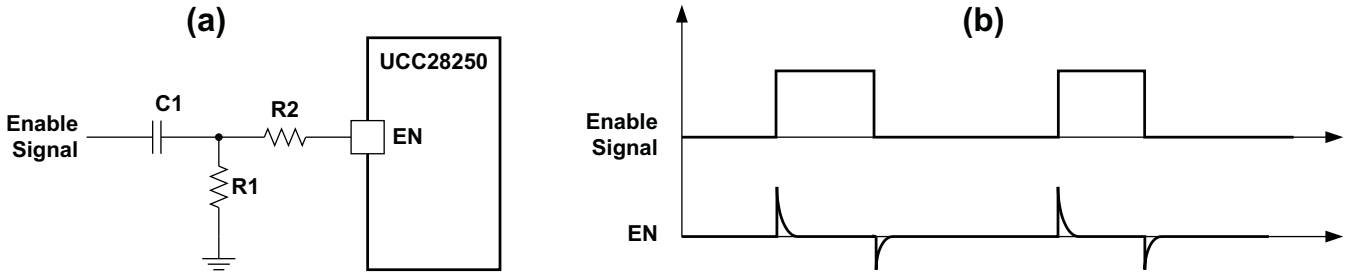


Figure 23. An External Solution to Generate Enable Pulses for Pulse Enable

Feature Description (continued)

7.3.4 RT (Oscillator Frequency Set and Synchronization) (15/2)

The UCC28250 oscillator frequency is set by an external resistor connected between the RT pin and ground. Switching frequency selection is a trade-off between efficiency and component size. Based on the selected switching frequency, the programming resistor value can be calculated as:

$$R_T = \frac{\frac{1}{2 \times f_{SW}} - T_{d(SP)}}{33.2\,pF} \quad (3)$$

In this equation, f_{SW} is the switching frequency and $T_{D(sp)}$ is the dead time between synchronous rectifier turnoff to primary switch turnon. $T_{D(sp)}$ is set by an external resistor between the SP pin and ground (refer to *SP (Synchronous Rectifier Turnoff to Primary Output Turnon Dead Time Programming) (13/19)*).

Each output (OUTA, OUTB, SRA, SRB) switches at half the oscillator frequency (f_{SW} = ½ x f_{OSC}). Figure 24 shows the relationship between RT and f_{OSC} at certain $T_{D(sp)}$ and can be used to program oscillator frequency accordingly.

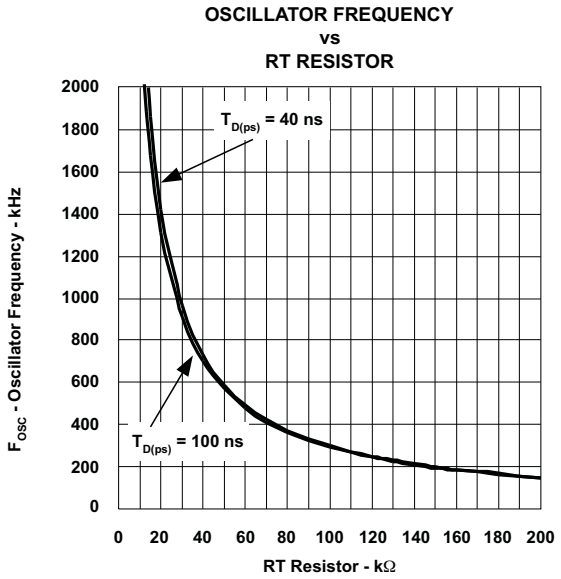


Figure 24. Oscillator Frequency F_{OSC} vs External Resistance of RT at $T_{D(ps)}$ = 40 ns and 100 ns

The UCC28250 can be synchronized to an external clock by applying an external clock source to the RT pin. Synchronization helps with parallel operation and/or preventing beat frequency noise. The UCC28250 synchronizes its internal oscillator to an external frequency source ranging from 170 kHz to 2.3 MHz, which is equivalent to an 85-kHz to 1.15-MHz switching frequency. The internal oscillator frequency is clamped to 170 kHz during synchronization if the external source frequency drops below 170 kHz.

The UCC28250 aligns the turnon of primary outputs OUTA and OUTB to the falling edge of the synchronizing signal, as shown in Figure 25. If the frequency source is from the gate outputs of another half bridge controller, interleaving can be achieved. The interleaving angle is determined by the frequency source's duty cycle. When a 50% duty cycle is applied, optimal interleaving is achieved, and EMI filters can be minimized.

Feature Description (continued)

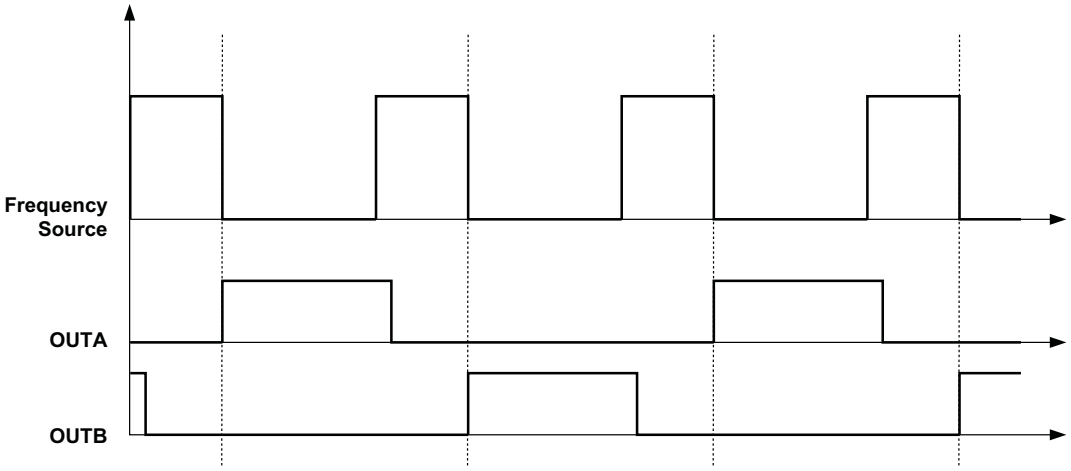


Figure 25. Timing Diagram for Synchronization

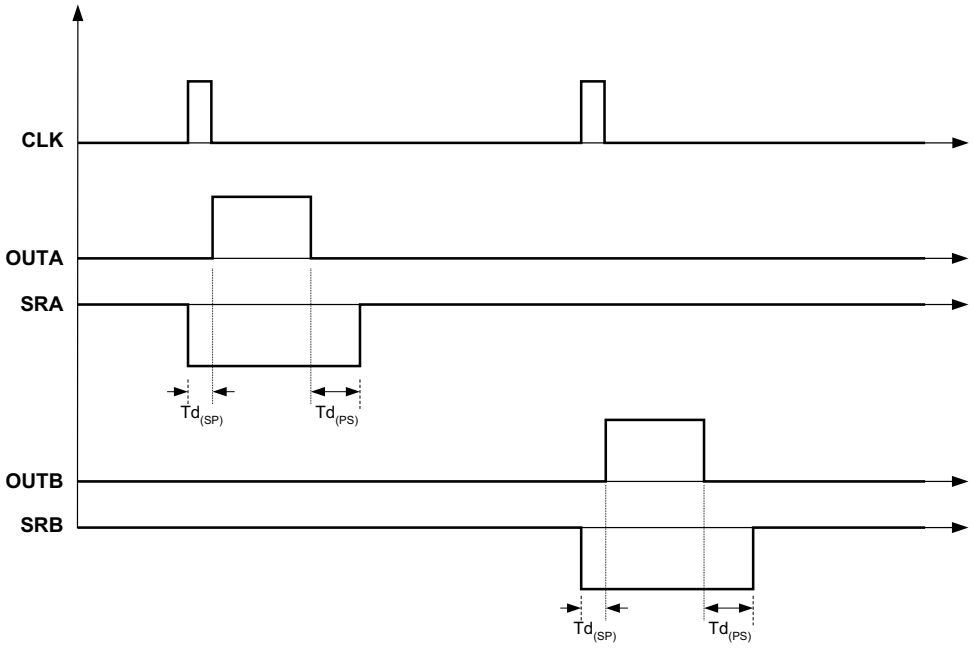


Figure 26. UCC28250 Outputs Timing Waveforms

Feature Description (continued)

7.3.5 SP (Synchronous Rectifier Turnoff to Primary Output Turnon Dead Time Programming) (13/19)

The dead time $T_{D(sp)}$ between synchronous rectifier turnoff to primary output turnon is programmed by an external resistor, R_{SP}, connected between the SP pin and ground. The value of R_{SP} can be determined by Figure 27. Zero dead time can be achieved by tying the SP pin to VREF. The falling edge of synchronous rectifier SRA/SRB is aligned with the raising edge of the primary output OUTA/OUTB.

NOTE

The minimum value for R_{PS}/R_{SP} is 5 kΩ and the maximum value is 250 kΩ.

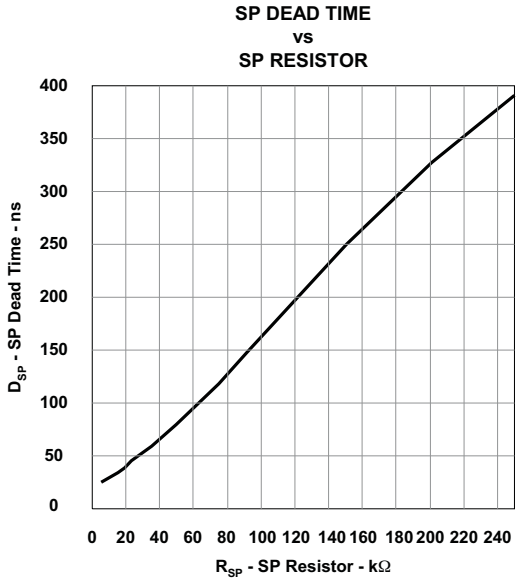


Figure 27. Dead Time $T_{D(sp)}$ vs. External Resistor R_{SP} at SP Pin

Feature Description (continued)

7.3.6 PS (Primary Output Turnoff to Synchronous Rectifier Turnon Dead Time Programming) (11/18)

The dead time $T_{D(ps)}$ between primary output turnoff to synchronous rectifier turnon is set by external resistor, R_{PS}, connected between PS pin and ground. The value of is R_{PS} is defined by Figure 28. Zero dead time can be achieved by tying the SP pin to VREF.

NOTE

The minimum value for R_{PS}/R_{SP} is 5 kΩ and the maximum value is 250 kΩ.

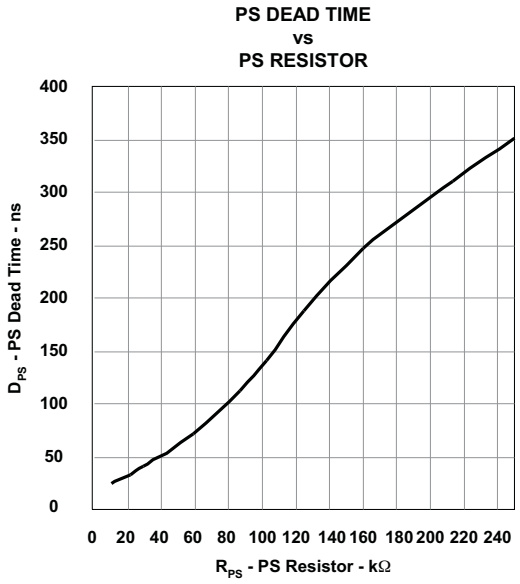


Figure 28. Dead Time $T_{D(ps)}$ vs. External Resistor R_{PS} at PS Pin

Feature Description (continued)

7.3.7 RAMP/CS (PWM Ramp Input or Current Sense Input) (16/3)

The UCC28250 can be controlled using either voltage mode or current mode. RAMP/CS is a multi-function pin used either to generate the ramp signal for voltage mode control or to sense current for current mode control.The following sections describe the RAMP/CS functionality for voltage mode and current mode control.

7.3.7.1 RAMP: Voltage Mode Control With Feed-Forward Operation

For voltage mode control, a resistor R_{CS} and a capacitor C_{CS} must be connected to the RAMP/CS pin as shown in Figure 29. The internal pulldown switch has approximately 40-Ω on-resistance. The RAMP/CS pin is clamped internally to 4 V for internal device protection. The C_{CS} value must be small enough to discharge the RAMP/CS pin from its peak voltage to ground within the pulse width of the BLANK signal ($T_{D(sp)}$ + 70 ns). The following formula derives a C_{CS} value.

$$C_{CS} < \left(\frac{4\,V/2}{40\,\Omega}\right) \times \frac{T_{d(SP)} + 70\,ns}{4\,V} \tag{4}$$

A C_{CS} value less than 650 pF works for most applications. To minimize the impacts of parasitic capacitance caused by the PCB layout and routing, a minimum of 100 pF is recommended for C_{CS}. Once C_{CS} is determined, R_{CS} can be calculated according to the desired ramp peak amplitude.

$$R_{CS} = \frac{1}{2 \times \ln\left(\frac{V_{CHARGE}}{V_{CHARGE} - V_{PK}}\right) \times C_{CS} \times f_{SW}} \tag{5}$$

In this equation, the V_{CHARGE} is the voltage used to generate the ramp, V_{PK} is the desired ramp amplitude and the f_{SW} is the switching frequency.

Choose the ramp amplitude to accommodate the voltage range of the COMP pin and the maximum duty cycle required by the power stage. Use the following equation to select V_{PK}, in the equation, D_{MAX} is the maximum duty cycle for primary outputs.

$$V_{PK} = \frac{1.4\,V}{D_{MAX}} \tag{6}$$

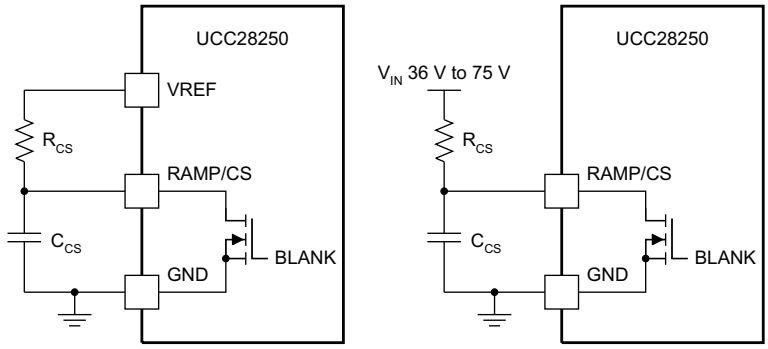


Figure 29. Fixed Ramp Generation/Ramp Generation With Input Voltage Feedforward

Voltage feed-forward can be achieved by driving R_{CS} from line input VIN. The peak of RAMP/CS is proportional to VIN and output has have much faster line transient response. When the UCC28250 is used for the primary-side control, RAMP parameters are critical for the optimal prebiased start-up performance. Refer to the *RAMP: Voltage Mode Control With Feed-Forward Operation* for a detailed design procedure of choosing R_{CS}.

If the line input cannot be easily accessed due to limited board area or other limitation, a RAMP signal with fixed peak voltage can be implemented by simply driving R_{CS} from 3.3-V VREF (Figure 29).

Feature Description (continued)

7.3.7.2 CS: Current Mode Control

For current mode control, the RAMP/CS pin is driven by a signal representative of the transformer primary-side current. The current signal must have compatible input range of the COMP pin. As shown in Figure 30, the COMP pin voltage is used as the reference for peak current. The primary-side signals OUTA and OUTB are turned on by the internal clock signal and turned off when sensed peak current reaches the COMP pin voltage. Choose the current sense transformer turns ratio (1:n) and the burden resistor value (R_B) based on the peak current at maximum load I_{MAX}.

$$R_B = \frac{3\,V}{I_{MAX}/n} \tag{7}$$

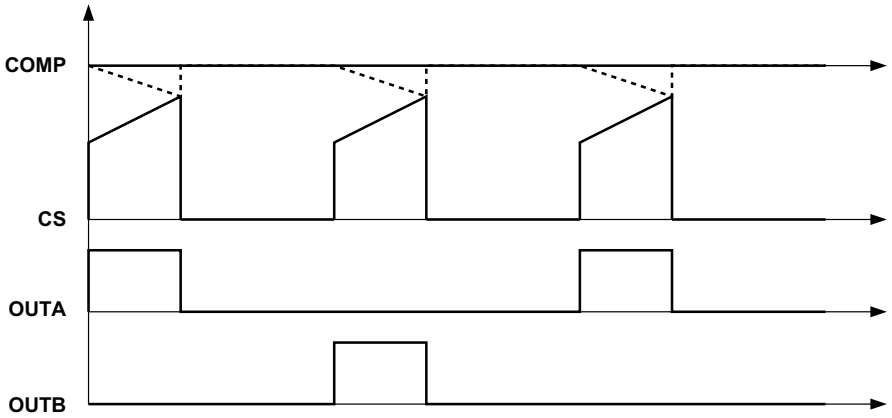


Figure 30. Peak Current Mode Control and PWM Generation

7.3.8 REF/EA+ (1/8)

REF/EA+ is the noninverting input of the UCC28250's internal error amplifier.

When the UCC28250 is configured for secondary-side control, the internal error amplifier is used as the control loop error amplifier. Connect REF/EA+ directly to the VREF pin to provide the reference voltage for the feedback loop.

When the UCC28250 is configured for primary-side control, the error amplifier is connected as a voltage follower. Connect REF/EA+ to the opto-coupler output.

The voltage range on REF/EA+ pin is 0 V to 3.7 V.

Feature Description (continued)

7.3.9 FB/EA- (2/9)

FB/EA- is the inverting input of the UCC28250's internal error amplifier.

When the UCC28250 is configured for secondary-side control, connect the output voltage sensing divider to this pin. The voltage divider can be selected according to the voltage on REF/EA+ pin. Referring to Figure 32, pick the lower resistor R_{O1} value arbitrarily, and choose the upper resistor R_{O2} value as:

$$R_{O2} = \left(\frac{V_O}{V_{REF/EA+}} - 1 \right) \times R_{O1} \tag{8}$$

Because the control loop gain is affected by voltage divider resistor values, choose an appropriate R_{O1} value so that the voltage loop DC gain is larger than 40 dB to prevent interference between the primary-side control loop and the SR control loop during start-up.

When the UCC28250 is sitting on the primary side, the error amplifier is connected as a voltage follower. Connect FB/EA- directly with COMP pin.

The maximum voltage allowed on FB/EA- pin is 3.7 V.

7.3.10 COMP (3/10)

The COMP pin is the internal error amplifier's output and also the input signal for PWM comparator. The maximum input common voltage of the PWM comparator is 2.8 V. It is suggested to program the peak value of RAMP to be lower than 2.3 V. Otherwise, the voltage of COMP pin should be clamped to be lower than 2.8 V by external circuit to make the internal PWM comparator work properly. Figure 31 shows tan external circuit that is recommended for voltage clamp function. Both the primary-side switches' duty cycle and secondary-side SRs' duty cycle is controlled by the COMP pin voltage. At steady state, a higher COMP pin voltage results in a larger duty cycle for the primary-side switches and a smaller duty cycle on the SRs.

When the UCC28250 controller is set up for secondary-side control, connect the compensation network from the FB/EA- pin to the COMP pin.

For primary-side control, the error amplifier is connected as a voltage follower. Directly connect the COMP pin to the FB/EA- pin.

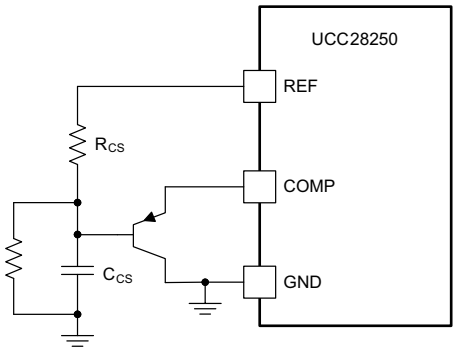


Figure 31. Comp Clamp Circuit

7.3.11 VSENSE (14/1)

The VSENSE pin is used to directly sense the output voltage and to feed it into a transconductance error amplifier. The measured voltage allows the UCC28250 to achieve optimal prebiased start-up performance.

When configured as a secondary-side controller, the output voltage is sensed and fed into the FB/EA- pin. The UCC28250 uses a conventional error amplifier approach to allow type III compensation. Therefore, the FB/EA- pin voltage always follows the REF/EA+ voltage. The FB/EA- pin does not reflect the true output voltage and therefore this dedicated VSENSE pin is required. The voltage divider connected to VSENSE is discussed in the Prebiased Start-Up Section.

When UCC28250 is set up as primary-side control, connect VSENSE pin to VREF.

Feature Description (continued)

7.3.12 SS (Soft Start Programming Pin) (13/20)

The soft-start circuit gradually increases the converter's output voltage until steady state operation is reached. This reduces start-up stresses and current surge.

When the UCC28250 reaches its valid operating threshold, the SS pin capacitor is charged with a 27-µA current source. The UCC28250's internal error amplifier noninverting terminal follows the SS pin voltage on REF/EA+ pin voltage depending on which one is lower. Hence, during soft start, the SS pin voltage is lower than REF/EA+. The internal error amplifier then uses the SS pin as its reference voltage, until the SS pin voltage rises above the REF/EA+ level. Once the SS pin voltage is above REF/EA+ voltage, soft-start time is considered finished.

The soft-start implementation scheme and timing is different, depending on the location of the UCC28250 with respect to the isolation barrier.

For secondary-side control, the internal error amplifier is used to achieve the voltage regulation. The REF/EA+ is connected to an external reference voltage, FB/EA- is connected to the voltage sensing divider, and the error amplifier's output pin (COMP) is connected through a compensation filter back to the FB/EA- pin (Figure 32). In this case, the primary output's start-up is a closed loop soft start (soft-start input reference of error amplifier). The output soft-start time is determined by the external capacitor connected at SS pin based on the internal 27-µA charging current and the voltage set at REF/EA+ pin.

Based on the soft-start time T_{SS}, choose soft start capacitor C_{SS} value as:

$$C_{SS} = \frac{27\,\mu A \times T_{SS}}{V_{REF/EA+}} \tag{9}$$

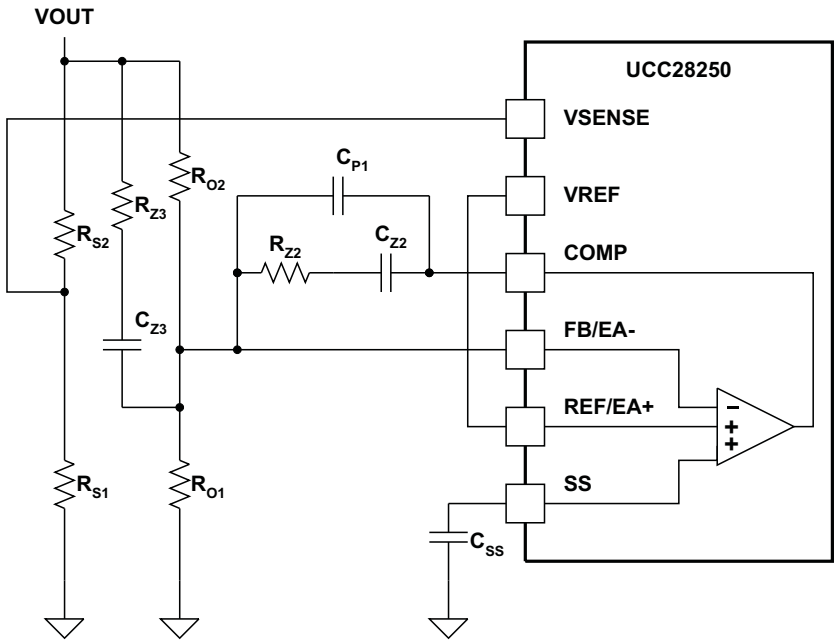


Figure 32. Error Amplifier EAMP Connections for Secondary-Side Control

Feature Description (continued)

For primary-side control, the internal error amplifier is connected as a buffer stage. In other words, the COMP pin is shorted to the FB/EA- pin, and the output of an external error amplifier is connected to the REF/EA+ pin through an optical coupler (Figure 33). In this case, the output start-up is an open loop soft start because the COMP follows the soft-start voltage instead of the voltage loop output. The soft-start time is still determined by external capacitor C_{SS} and the 27-µA internal charge current. The voltage depends on the value of final COMP voltage which corresponds to the regulated primary output duty cycle. According to the desired soft start time and COMP pin voltage level at steady state, the SS pin capacitor can be calculated as:

$$C_{SS} = \frac{27\,\mu A \times T_{SS}}{V_{COMP\_final}} \tag{10}$$

After soft start, the voltage at SS pin is eventually clamped at around 4 V. Under fault conditions (UVLO, internal thermal shut down, OVP/OTP, hiccup mode), or when externally disabled, SS pin is pulled down to ground quickly by an internal switch with 2 kΩ on resistance to prepare for re-start. Pulling SS pin to ground externally shuts down the controller as well.

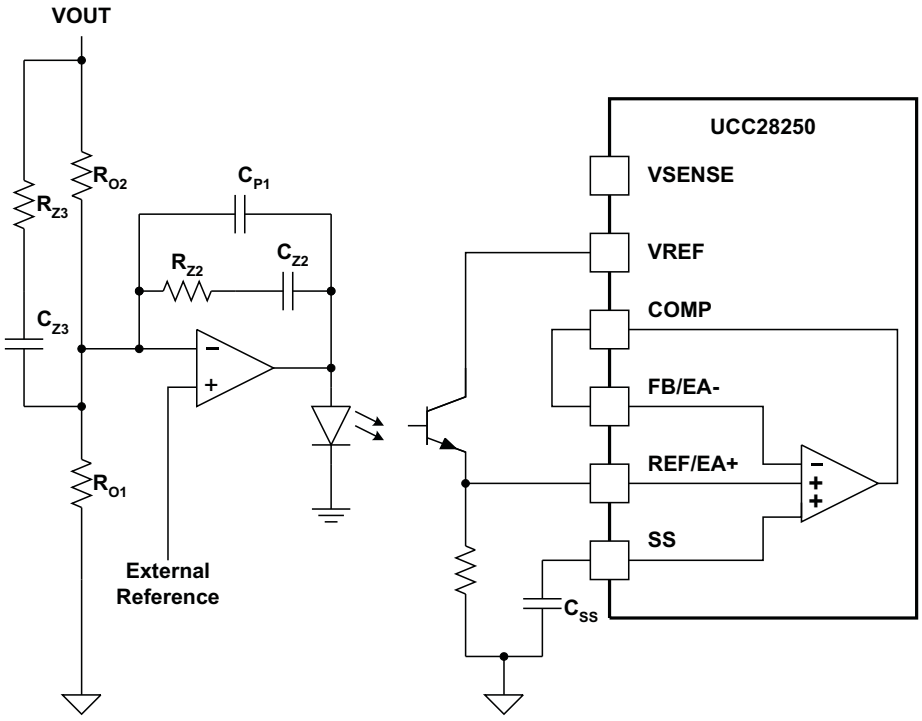


Figure 33. Error Amplifier EAMP Connections for Primary-Side Control

Feature Description (continued)

7.3.13 ILIM (Current Limit for Cycle-By-Cycle Overcurrent Protection) (17/4)

Cycle-by-cycle current limit is accomplished using the ILIM pin for current mode control or for voltage mode control. The input to the ILIM pin represents the primary current information. If the voltage sensed at ILIM pin exceeds 0.5 V, the current sense comparator terminates the pulse of output OUTA or OUTB. If the high current condition persists, the controller operates in a cycle-by-cycle current limit mode with duty cycle determined by the current sense comparator instead of the PWM comparator. ILIM pin is pulled down by an internal switch at the rising edge of every clock cycle. This internal switch remains on for an additional 70 ns after OUTA or OUTB goes high to blank leading edge transient noise in the current sensing loop. This reduces the filtering requirements at the ILIM pin and improves the current sense response time.

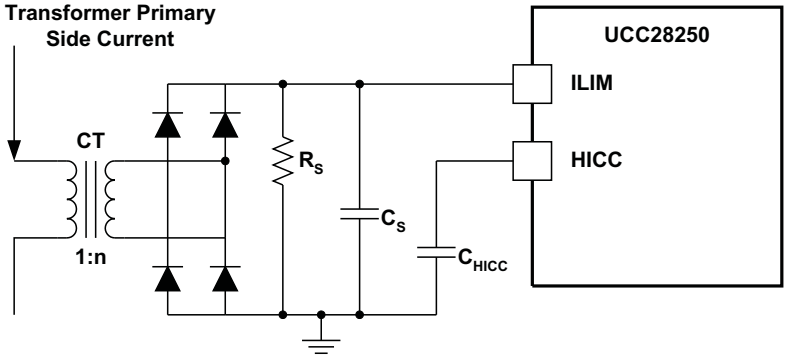


Figure 34. Current Limit Circuit

Once the over current protection level I_{PK} is selected, the current transformer turns ratio and the burden resistor value can be decided as:

$$R_S = \frac{0.5\,V \times n}{I_{PK}} \tag{11}$$

In this equation, current transformer turns ratio is 1:n and R_S is the burden resistor value.

Some filtering capacitance is required to reduce the sensing noise. Choose the RC constant at about 100 ns, and calculate the capacitor value as:

$$C_S = \frac{100\,ns}{R_S} \tag{12}$$

The cycle-by-cycle current limit operation time before all four outputs shut down can be programmed by external capacitor C_{HICC} at HICC pin. (See HICC pin description)

Feature Description (continued)

7.3.14 HICC (10/17)

The cycle-by-cycle current limit operation time before all four outputs shut down can be programmed by an external capacitor C_{HICC} from HICC pin to ground, as shown in Figure 34. Once all four outputs are shutdown, controller goes into hiccup cycle which is about 100 times of the cycle-by-cycle current limit shut-down delay time. A 1-mA internal current source charges HICC pin up to 2.4 V, then the HICC pin is discharged by a 2.7-µA internal current source to generate long hiccup restart time until HICC reaches 0.3 V. Based on the system requirement, once the cycle-by-cycle current limit delay time $T_{OC(delay)}$ is selected, the HICC pin capacitor C_{HICC} can be selected based on the equation

$$C_{HICC} = \frac{T_{OC(delay)} \times 75\,\mu A}{0.6\,V} \tag{13}$$

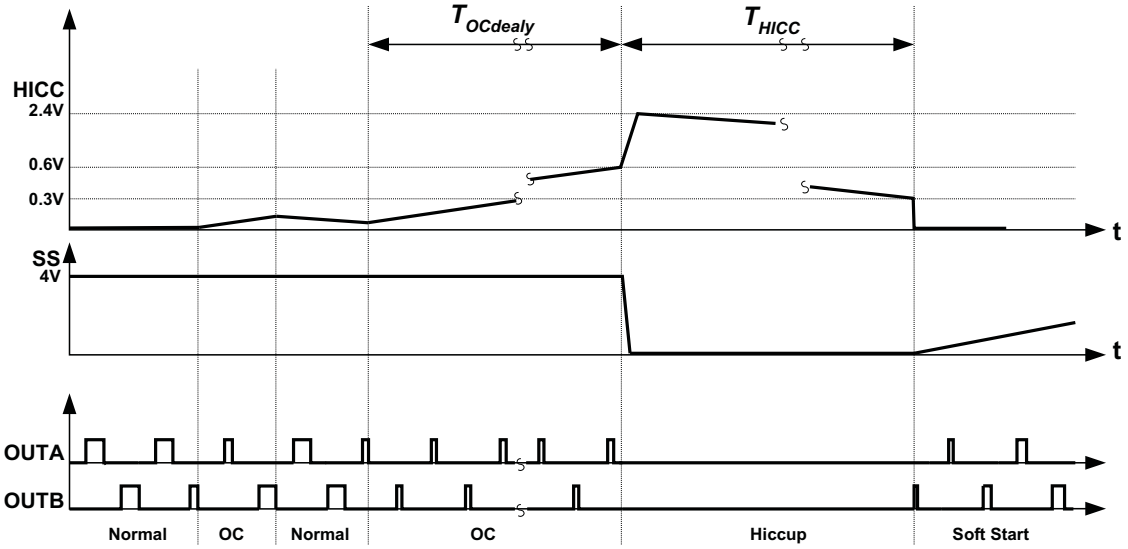


Figure 35. Cycle-by-Cycle Current Limit Delay Timer and Hiccup Restart Timer

As shown in Figure 35, cycle-by-cycle current limiting shut-down delay time is:

$$T_{OC(delay)} = C_{HICC} \times \frac{0.6\,V}{75\,\mu A} \tag{14}$$

And hiccup-restart-time T_{HICC} is equal to:

$$T_{HICC} = C_{HICC} \times \frac{2.4\,V - 0.3\,V}{2.7\,\mu A} \tag{15}$$

As soon as the outputs are shut-down, the SS pin is pulled to ground internally until the hiccup restart timer is reset after time duration T_{HICC}.

Feature Description (continued)

7.3.15 OVP/OTP (19/6)

The OVP/OTP pin provides multiple fault protection functions. If the voltage on the OVP/OTP pin exceeds 0.7 V, a fault shutdown occurs. All outputs stop switching and stay off (low) during the shutdown, and the SS pin is pulled to ground internally. Once the fault condition is cleared (that is, OVP/OTP voltage drops below 0.7 V), the UCC28250 enters hiccup mode. A soft-start cycle begins after the hiccup cycle is finished. An internal 11-µA switched current source is used to create hysteresis.

If the external resistor divider runs from line voltage VIN, a line overvoltage protection is implemented.

If the external resistor divider runs from the output voltage, output overvoltage fault protection is achieved. Figure 36 shows the overvoltage protection external configuration at the OVP/OTP pin.

According to the protection threshold V_R and recovery threshold V_F, choose an arbitrary R_2 value. To ensure a realistic solution, R_2 must meet the following:

$$R_2 < \frac{0.7\,V \times (V_R - V_F)}{11\mu A \times (V_R - 0.7\,V)} \tag{16}$$

The other two resistors, R_1 and R_3 can be calculated.

$$R_1 = \frac{V_R - 0.7\,V}{0.7\,V} \times R_2 \tag{17}$$

$$R_3 = \frac{0.7\,V \times (V_R - V_F) - 11\mu A \times R_2 \times (V_R - 0.7\,V)}{11\mu A \times V_R} \tag{18}$$

If the external resistor divider runs from 3.3-V VREF, and replaces R_2 with a positive temperature coefficient (PTC) thermistor, an overtemperature fault protection with programmable hysteresis is accomplished (Figure 37). Choose an arbitrary PTC value, which has a resistance as R_{PTC1} at protection temperature and resistance as R_{PTC2} at recovery temperature. Because of its positive temperature coefficient, R_{PTC1} is larger than R_{PTC2}. To ensure an available solution, R_{PTC1} and R_{PTC2} need to meet the criteria.

$$0.7\,V \times (R_{PTC1} - R_{PTC2}) - 11\mu A \times R_{PTC1} \times R_{PTC2} \geq 0 \tag{19}$$

And resistors R_1 and R_3 can be calculated as:

$$R_1 = 3.7 \times R_{PTC1} \tag{20}$$

$$R_3 = \frac{2.6\,V \times \left[0.7\,V \times (R_{PTC1} - R_{PTC2}) - 11\mu A \times R_{PTC1} \times R_{PTC2}\right]}{11\mu A \times (2.6\,V \times R_{PTC1} + 0.7\,V \times R_{PTC2})} \tag{21}$$

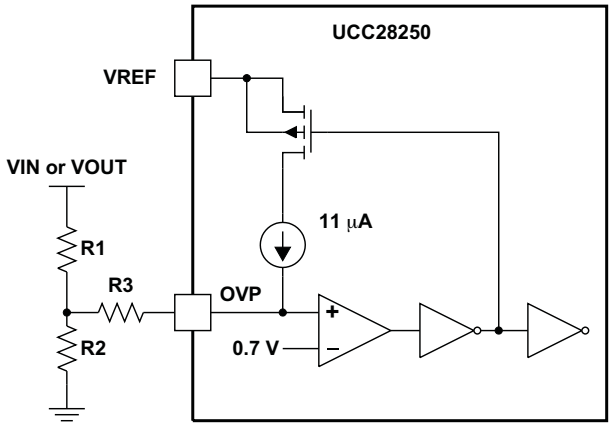


Figure 36. Overvoltage Protection

Feature Description (continued)

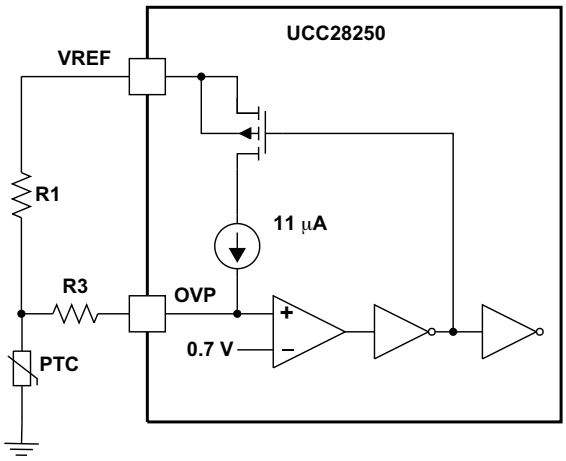


Figure 37. Overtemperature Protection

Figure 38 shows an external configuration using the OVP/OTP pin to achieve both overvoltage and overtemperature protection. Follow the same design procedure for the OVP setting to choose R_1, R_2, and R_3. Choose an NTC value at protection temperature much smaller than R_1 and with the resistance at protection temperature as R_{NTC1}, and recover temperature as R_{NTC2}. The R4 value can be calculated as:

$$R_4 = \frac{0.7\,V}{3.3\,V - 0.7\,V} \times R_{NTC1} \tag{22}$$

Because of the interaction between the two voltage dividers, overtemperature protection thresholds move slightly with the different input voltages.

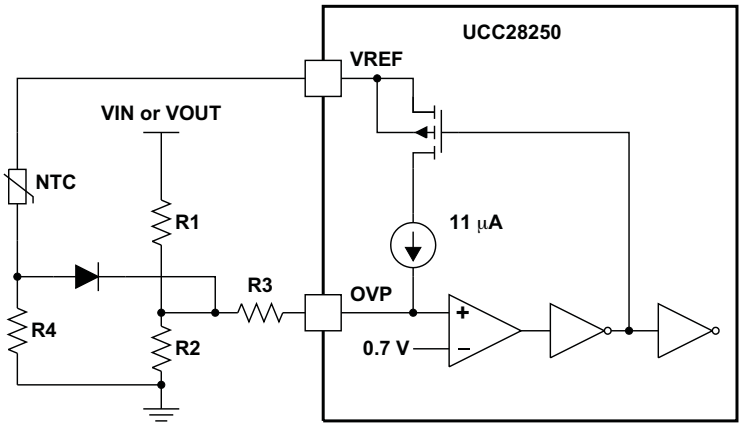


Figure 38. Overvoltage and Overtemperature Protection With Single OVP Pin

7.3.16 OUTA (9/16) and OUTB (8/15)

OUTA and OUTB are the primary-side switch control signals. With the 0.2-A peak current capability, an external gate driver is required.

7.3.17 SRA (7/14) and SRB (6/13)

SRA and SRB are the synchronous rectifier control signals. With the 0.2-A peak current capability, an external gate driver is required.

Feature Description (continued)

7.3.18 GND (4/11)

GND pin is the ground reference for the whole device. Tie all the signal returns to this pin.

7.4 Device Functional Modes

The UCC28250 can be controlled using either voltage mode or current mode. RAMP/CS is a multi-function pin used either to generate the ramp signal for voltage mode control or to sense current for current mode control. Refer to *RAMP/CS (PWM Ramp Input or Current Sense Input) (16/3)* for the details.

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCC28250 is a high-performance PWM controller with advanced synchronous rectifier outputs and is ideally suited for regulated half-bridge, full-bridge and push-pull converters. A dedicated internal prebiased start-up control loop working in conjunction with a primary-side voltage loop achieves monotonic prebiased start-up for either primary-side or secondary-side control applications. The UCC28250 architecture allows either voltage mode or current mode control.

Input voltage feedforward can be implemented, allowing PWM ramp generator to improve the converter line transient response. Advanced cycle-by-cycle current limit achieves volt-second balancing even during fault conditions. The hiccup timer helps the system to stay within a safe operation range under over load conditions. With a multifunction OVP/OTP pin, combinations of input voltage protection, output voltage protection and overtemperature protection can be implemented. The UCC28250 allows individual programming of dead time between primary-side switch and secondary-side SRs, To allow optimal power stage design. Dead time can also be reduced to zero, and this allows optimal system configuration considering the delays on the gate driver stage. The UCC28250 also provides complete system level protection functions, including UVLO, thermal shut down and overvoltage, overcurrent protection.

8.1.1 Error Amplifier and PWM Generation

The UCC28250 includes a high-performance internal error amplifier with low input offset, high source/sink current capability and high gain bandwidth (typical 3.5 MHz). The reference of the error amplifier (REF/EA+ pin) is set externally to support flexible trimming of the voltage loop, and to make the controller flexible for both primary side, as well as secondary-side control. The extra positive input for the error amplifier is the SS pin which is used to externally program the soft-start time of the converter's output.

During steady state operation, the primary switch duty cycle, D, is generated based on the external ramp on RAMP/CS pin and the COMP pin voltage. A higher COMP pin voltage results in a larger duty cycle. The secondary-side SR duty cycle is SR_D = (1-D), complementary to the primary-side duty cycle, without considering the dead time between primary-side switch and secondary-side SR. The primary outputs begin to switch when COMP pin voltage is above the 350 mV internal offset. The synchronous rectifier outputs only switch after COMP pin voltage is above 550 mV internal offset. According to the internal logic, the minimum pulse width for the primary-side OUTA and OUTB is typically 100 ns.

During soft start, the primary-side switch duty cycle is generated based on the external ramp on RAMP/CS pin and the COMP pin voltage. However, the duty cycle of secondary-side SR is generated based on an internal ramp and the COMP pin voltage. When the converter is controlled on the primary side, an internal ramp is a fixed ramp with 3-V peak voltage. When the converter is controlled on secondary side, an internal ramp is generated based on the internal prebiased start-up loop. An internal prebiased start-up loop modifies the SR duty cycle during soft start to achieve the optimal prebiased start-up performance.

After the SS pin reaches 2.9 V, the prebiased start-up control loop is disabled. The secondary-side SR instantaneously changes into its steady state value as complementary to the primary-side duty cycle.

8.1.2 Prebiased Start-Up

With the internal error amplifier, UCC28250 supports both primary-side control and secondary-side control. For different control methods, the controller is configured accordingly and so is the prebiased start-up control. During soft start, both the primary-side switches' duty cycle and secondary-side SRs' duty cycle are increased. This gradually increases the output voltage until steady state operation is reached, thereby reducing surge current.

Application Information (continued)

8.1.2.1 Secondary-Side Control

For secondary-side control, the UCC28250 implements close-loop control of both the primary-side switches and secondary-side synchronous rectifiers' duty cycles. This makes it easy to achieve optimal start-up performance.

The internal error amplifier is set up as the control loop error amplifier. Connect REF/EA+, FB/EA-, COMP and VSENSE as shown in Figure 39. To achieve optimal prebiased start-up performance, the output voltage must be directly measured. The UCC28250 uses the VSENSE pin to directly sense this output voltage. Choose the voltage dividers on VSENSE slightly different to the FB/EA- voltage divider so that the voltage on VSENSE pin is roughly 10% to 15% more than FB/EA- pin voltages. Select R_{O1} equal to R_{S1}, and R_{S2} about 10% to 15% smaller than R_{O2}.

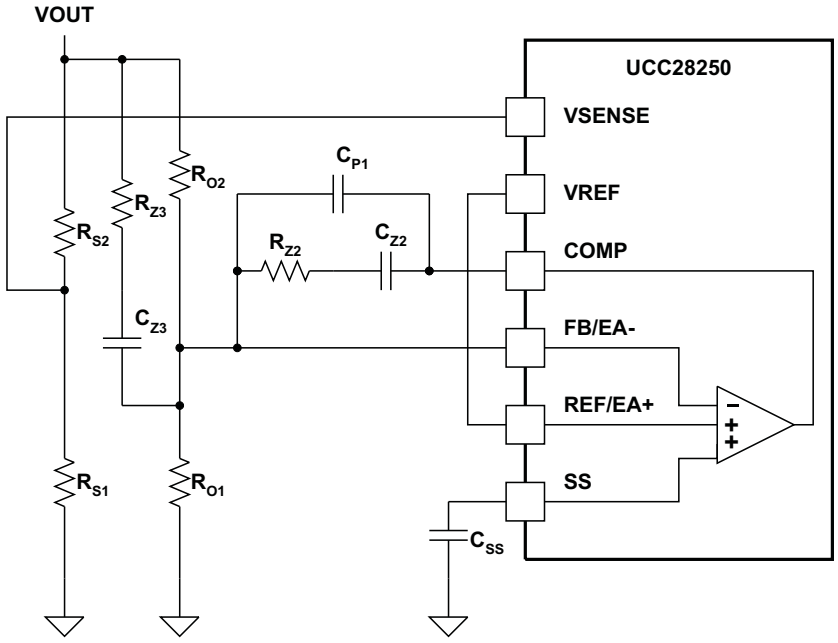


Figure 39. Error Amplifier Set Up for Secondary-Side Control

The error amplifier uses the lower voltage between the SS pin and the REF/EA+ pin to be the reference voltage for the feedback loop. In this method, the control loop is said to be 'closed' during the entire start-up process, as it is always based on the true output voltage.

During soft start, the primary-side switch duty cycle is controlled by the COMP pin voltage and ramp voltage generated on the RAMP/CS pin. A higher COMP pin voltage results in larger duty cycle. However, to improve start-up performance, the secondary-side synchronous rectifier duty cycle is controlled by a separate, internal ramp signal (generated by a dedicated prebiased start-up loop) and by the COMP pin voltage. This dedicated prebiased loop is much faster than the regular voltage loop to avoid interaction between the two loops. The start-up loop reads the output voltage through a transconductance error amplifier connected to the VSENSE pin. When the output voltage is higher than the reference, the prebiased start-up loop increases the SR duty cycle to reduce the output voltage. Conversely, when the output voltage is lower than the reference, the SR duty cycle is decreased to help maintain higher output voltage. To speed up the start-up time, the minimum duty cycle of the synchronous rectifier is 50%.

Once the soft start is finished, the prebiased loop is disabled and the duty cycle of the synchronous rectifiers becomes the complimentary of primary switches' duty cycle, with some dead time inserted in between.

Application Information (continued)

8.1.2.2 Primary-Side Control

When the UCC28250 is sitting on the primary side, the internal error amplifier is connected as a voltage follower and an extra error amplifier is needed on the secondary side for closed loop control. The error amplifier implementation is shown in Figure 40.

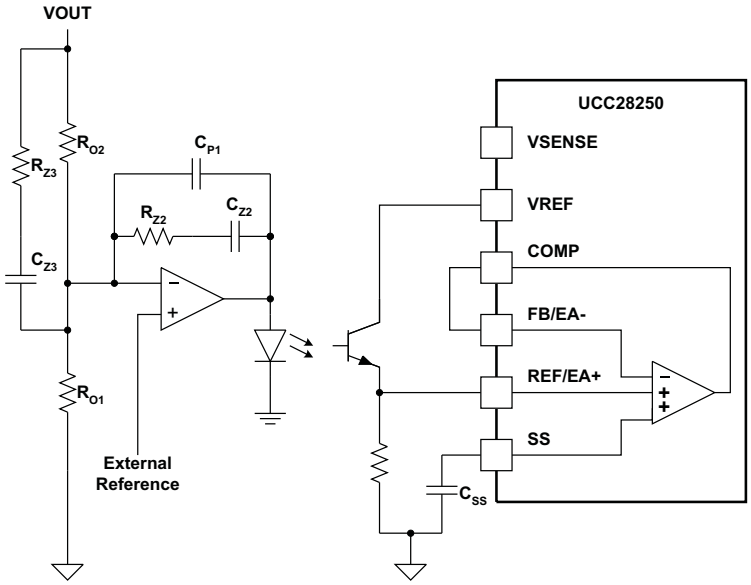


Figure 40. Error Amplifier Setup for Primary-Side Control

In the above configuration, the UCC28250 can only see the control loop feedback voltage, and cannot directly access the output voltage. The design of the soft-start time is critical to achieve optimal prebiased start-up performance. Some trial and error approaches are needed to achieve optimal performance. It is also important to choose the appropriate ramp amplitude. Refer to *RAMP/CS (PWM Ramp Input or Current Sense Input) (16/3)* discussion on the detailed design procedure for choosing ramp generation components.

During soft start, regardless of the prebiased condition, the output voltage is always lower than the regulation voltage, so that the feedback loop is always saturated. When the internal error amplifier is connected as a voltage follower, the COMP voltage follows the lower of the voltage on the RER/EA+ pin and the SS pin. Because the feedback loop is saturated, the COMP pin always follows the SS pin voltage, until the output voltage becomes regulated and the feedback voltage takes over. In this control method, the output voltage control loop is always saturated, and the controller soft starts the COMP pin voltage. Therefore, it is called open loop soft start.

The primary-side switch duty cycle is controlled by the COMP pin voltage and by the RAMP/CS pin voltage. During soft start, the COMP pin voltage follows the SS pin as it is rising, so the primary-side switch duty cycle keeps increasing. When the output voltage becomes regulated, the feedback voltage becomes less than the SS pin voltage and the primary-side switch comes controlled by the control loop.

For the primary-side control setup, because output voltage is not directly accessible, the internal prebiased start-up loop is disabled by connecting VSENSE to VREF. Instead, the internal ramp used to generate the synchronous rectifier duty cycle is fixed, with the peak voltage of 3 V. The duty cycle of the synchronous rectifier increases as the SS pin voltage increases. When the SS pin voltage reaches 2.9 V, the soft start is considered finished and the synchronous rectifier duty cycle becomes the complementary of the primary-side switch duty cycle, minus the programmed dead time. Because of different COMP pin voltages at different line voltages, the SR duty cycle generated by the internal ramp might be different than the complementary of the primary-side switch duty cycle (1-D). If the duty cycle is too large, the internal logic is able to limit the duty cycle to (1-D). However, if the duty cycle is too small, when the soft start is finished, the SR duty cycle has a sudden change, which will cause output voltage disturbance. To optimize the prebiased start-up performance, TI recommends that the duty cycle change at the end of soft start be as small as possible.

Application Information (continued)

8.1.2.3 Voltage Mode Control and Input Voltage Feed-Forward

For voltage mode control, a resistor R_{CS} and a capacitor C_{CS} are connected externally at RAMP/CS pin as shown in Figure 41. A ramp signal is generated on the RAMP/CS pin, at a rate of two times that of the switching frequency. The generated ramp signal is used to control the duty cycle for both the primary-side switches and secondary-side synchronous rectifiers. The ramp amplitude can be fixed or variable with the input voltage (input voltage feedforward).

To realize a fixed amplitude ramp, connect R_{CS} to the VREF pin, so that the ramp capacitor charging voltage is fixed regardless of line and load condition. The RAMP/CS pin is clamped internally to 4 V for internal device protection. Because the internal pulldown switch has about 40-Ω on-resistance, the C_{CS} value must be small enough to discharge RAMP/CS from the peak to ground within $T_{D(sp)}$ + 70 ns (that is, the pulse width of BLANK signal).

To achieve the input voltage feedforward, the slope of the ramp must be proportional to the input voltage. Tie R_{CS} to the input line voltage. Because the ramp voltage is much lower than the input voltage, the ramp capacitor charging current is considered to be proportional to the input voltage. With input voltage feedforward, the COMP pin voltage should only move slightly even with large input voltage variation. This will provide much better line transient response for the converter.

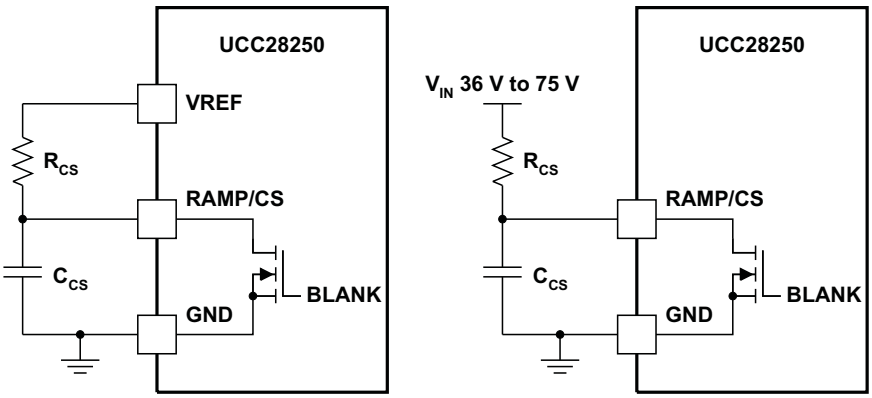


Figure 41. External Configuration of RAMP/CS Pin With/Without Feed-Forward Operation

Application Information (continued)

The input voltage feedforward also helps on prebiased start-up. When doing primary-side control to prebiased start-up, three conditions need to be considered:

8.1.2.3.1 Condition 1

At initial start-up, the primary side must provide enough energy to prevent output voltage dip;

8.1.2.3.2 Condition 2

At the end of soft start, it is required to keep the SR duty cycle change to be as small as possible. With input voltage feedforward, the COMP pin voltage is virtually fixed for different input voltages. Therefore, before the end of soft start, the duty cycle is the same for different input voltages. Choose the R_{CS} and C_{CS} following the procedure.

Considering initial start-up, the RAMP peak voltage should be:

$$V_{RAMP} = \frac{\frac{V_{IN}}{2 \times n} - V_{PRE-BIAS}}{2 \times V_{PRE-BIAS}} \times V_{SR(ramp)} \quad (23)$$

In this equation, VIN is the input voltage because of the feedforward any input voltage should be fine; $V_{PRE-BIAS}$ is the highest prebias start-up voltage required by the system; n is the tranformer primary to secondary turns ratio and $V_{SR(ramp)}$ is the internal SR ramp peak voltage 3 V.

Another consideration is at the end of soft start, the SR duty cycle changes from controlled by the soft start, to complimentary to the primary-side duty cycle. The design should keep the transition as smooth as possible. Considering this, based on the output voltage and input voltage range, as well as the transformer turns ratio, calculate the SR duty cycle at different line voltages.

Next, based on the maximum duty cycle on the SR_D_{MAX}, and the internal fixed ramp amplitude 3 V, the COMP voltage at regulation can be chosen as:

$$V_{COMP(final)} = (SR\_D_{MAX} - 0.5) \times 3\,V \times 2 \quad (24)$$

8.1.2.3.3 Condition 3

Use the calculated COMP pin voltage to derive the external ramp amplitude

$$V_{RAMP} = \frac{V_{COMP(final)}}{(1 - SR\_D_{MAX}) \times 2} \quad (25)$$

According to the calculated ramp voltage from Equation 23 and Equation 25 some trade off is required to pick up the appropriate ramp voltage. Based on the selected ramp capacitor C_{CS} value, choose the ramp resistor R_{CS} value:

$$R_{CS} = \frac{V_{IN(max)} \times 2}{V_{RAMP} \times C_{CS} \times f_{sw}} \quad (26)$$

In this equation, $V_{IN(max)}$ is the maximum input voltage, f_{SW} is the switching frequency.

Because these calculations ignore the dead time and the non-linearity of the ramp, slight modification is expected to achieve the optimal design. When the input voltage feed forward is not used, refer to *RAMP/CS (PWM Ramp Input or Current Sense Input) (16/3)* for RC calculation.

Application Information (continued)

8.1.2.4 Peak Current Mode Control

For peak current mode control, RAMP/CS pin is connected directly with the current signal generated from a current transformer. The current signal must be compatible with the input range of the COMP pin. External slope compensation is required to prevent sub-harmonic oscillation and to maintain flux-balance. The slope compensation can be implemented by using OUTA and OUTB to charge external capacitors and use the voltage follower to add into the sensed the current signal, as shown in Figure 42. Follow the peak current mode control theory to select compensation slope or refer to *Modeling, Analysis and Compensation of the Current-Mode Converter*, (SLUA101).

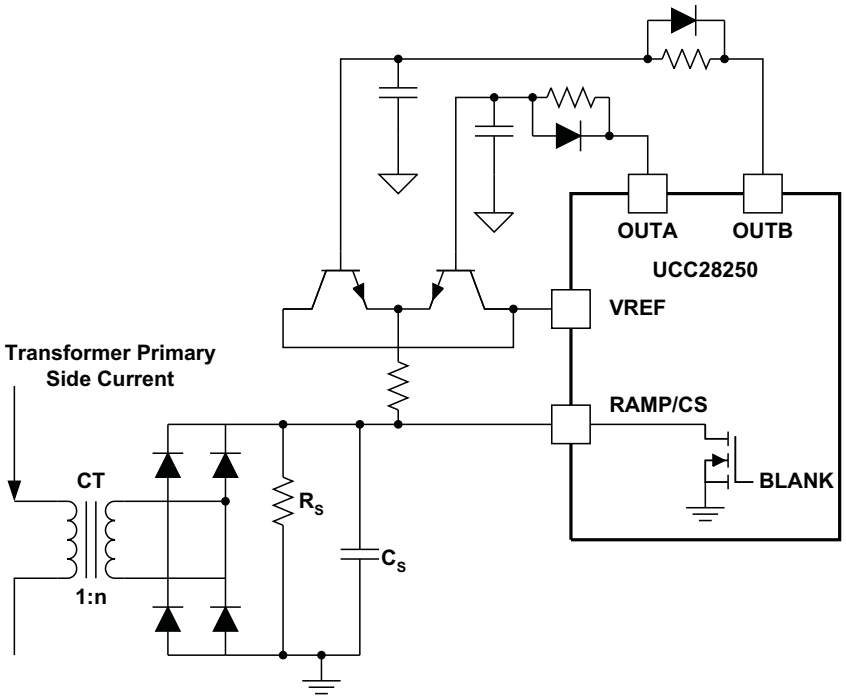


Figure 42. UCC28250 Set Up for Peak Current Mode Control

Application Information (continued)

8.1.2.5 Cycle-by-Cycle Current Limit and Hiccup Mode Protection

Cycle-by-cycle current limit is accomplished using the ILIM pin for both current mode control and voltage mode control. The input to the ILIM pin represents the primary current information. If the voltage sensed at ILIM pin exceeds 0.5 V, the current sense comparator terminates the pulse of output OUTA or OUTB. If the high current condition persists, the controller operates in a cycle-by-cycle current limit mode with duty cycle determined by the current sense comparator instead of the PWM comparator. ILIM pin is pulled down by an internal switch at the rising edge of each clock cycle. This internal switch remains on for an additional 70 ns after OUTA or OUTB goes high to blank leading edge transient noise in the current sensing loop. This reduces the filtering requirements at the ILIM pin and improves the current sense response time.

UCC28250 makes it possible to maintain flux balance during cycle-by-cycle current limit operation. The duty cycles of primary switches are always matched. If one switch duty cycle is terminated earlier because of current limiting, a matched duty cycle is applied to the other switch for the next half switching cycle, regardless of the current condition, as shown in Figure 43. This matched duty cycle helps to maintain volt-second balancing on the transformer and prevents the transformer saturation.

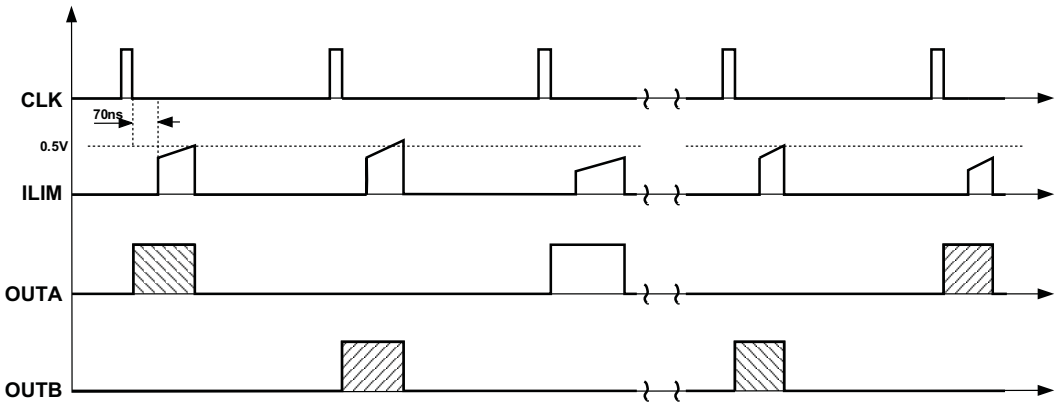


Figure 43. Cycle-by-Cycle Current Limit Duty Cycle Matching

Once the current limit is triggered, the 75-µA internal current source begins to charge the capacitor on HICC pin. If the current limit condition went away before HICC pin reaches 0.6 V, the device stops charge HICC capacitor and begins to discharge it with 2.7-µA current source. If the cycle-by-cycle current limit condition continues, HICC pin reachs 0.6 V, and all four outputs are shut down. The UCC28250 then enters hiccup mode. During hiccup mode, all four outputs keep low; SS pin is pulled to ground internally; a 2.7-µA current source continuously discharge HICC pin capacitor; until HICC pin voltage reaches 0.3 V. After that, HICC pin is discharged internally to get ready for the next HICC event. The whole converter starts with soft start after hiccup mode.

Application Information (continued)

The cycle-by-cycle current limit operation time before all four outputs shut down is programmed by external capacitor C_{HICC} at HICC pin. The delay time can be calculated as:

$$T_{OC(delay)} = C_{HICC} \times \frac{0.6\,V}{75\,\mu A} \quad (27)$$

The hiccup timer keeps all outputs being zero until the timer expires. The hiccup time T_{HICC} is calculated as:

$$T_{HICC} = C_{HICC} \times \frac{2.4\,V - 0.3\,V}{2.7\,\mu A} \quad (28)$$

As soon as the outputs are shut-down, SS pin is pulled down internally until the hiccup restart timer is reset after time duration T_{HICC}. The detailed illustration of HICCUP mode is shown in Figure 44.

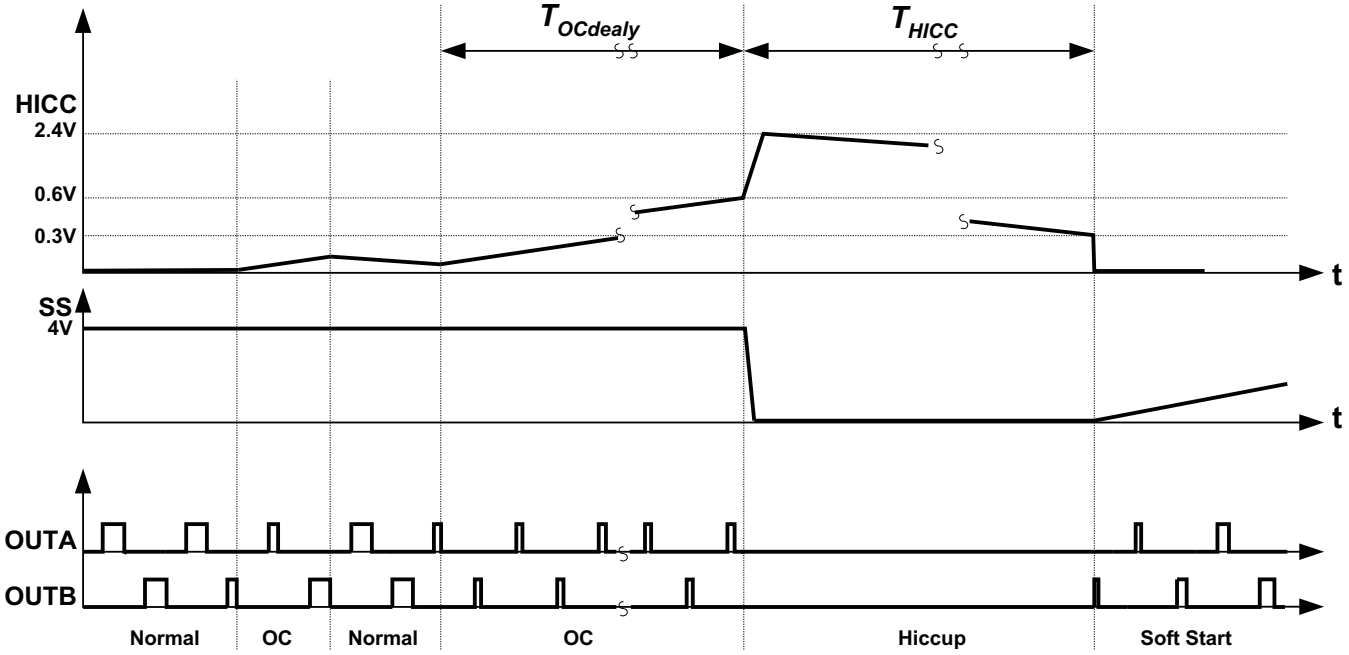


Figure 44. Cycle-by-Cycle Current Limit Delay Timer and Hiccup Restart Timer

8.2 Typical Applications

8.2.1 Design Example

The example provided shows how to design a symmetrical half bridge converter of voltage mode control with UCC28250 on primary side.

Figure 45 is the circuit diagram to be used in this design example. This design example shows how to determine the values in the circuit associated to UCC28250 programming.

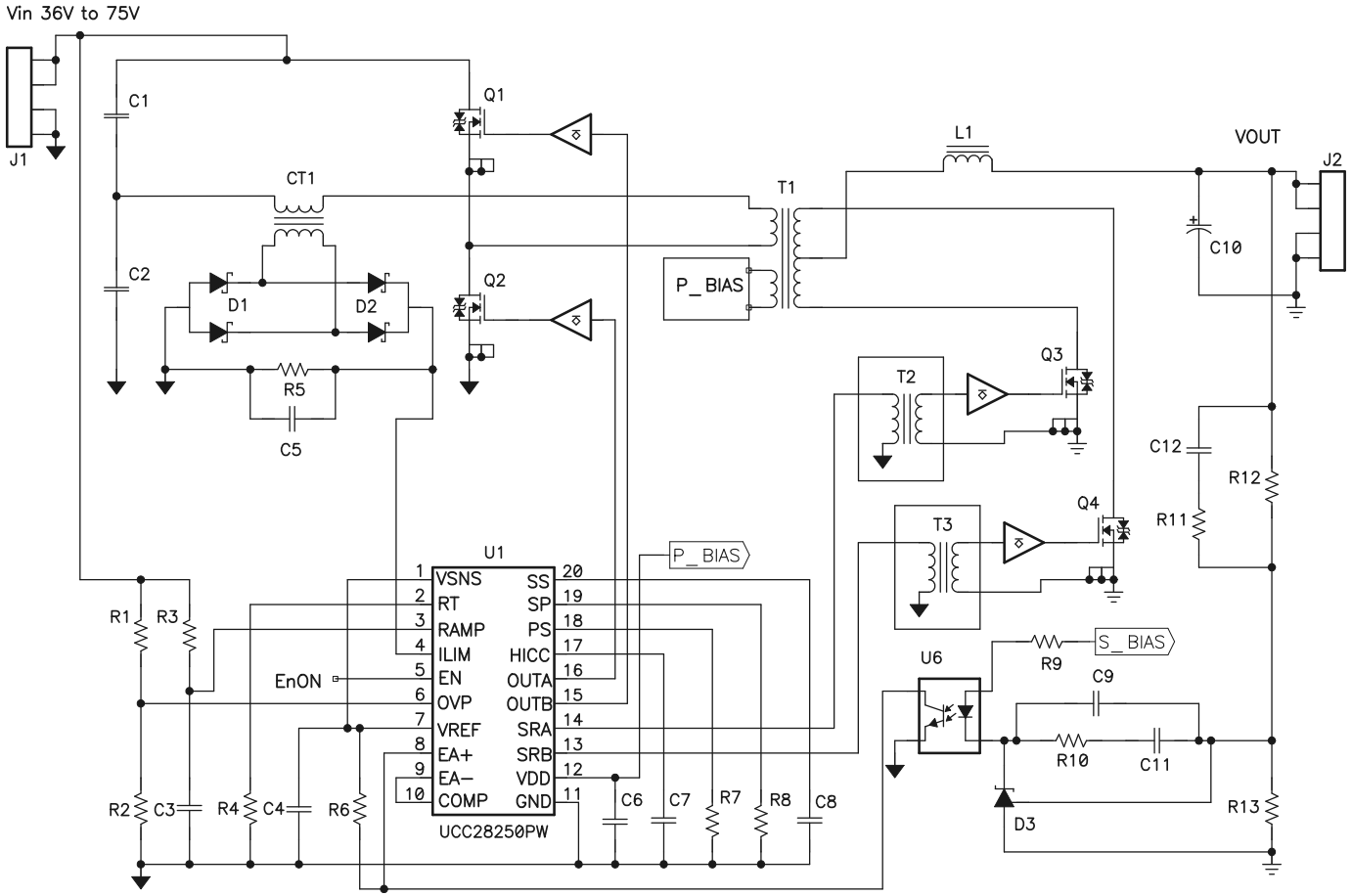


Figure 45. Circuit Diagram in Design Example

8.2.1.1 Design Requirements

Table 1 shows the specifications for the design example.

Table 1. Specifications for the Design Example

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	36	48	72	VDC
V_{OUT}	Output voltage		3.3		VDC
P_{OUT}	Output power			75	W
I_{OUT}	Output load current			23	A
C_{OUT}	Load capacitance			5000	µF
f_{SW}	Switching frequency		150		kHz
P_{LIMIT}	Over-power limit			150%	
η	Efficiancy at full load		90%		
	Isolation	1500			V

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Step 1, Power Stage Design

The power stage design in this example is standard and the same as that for symmetrical half bridge converter of voltage mode control. From the standard design, these components are determined. This includes Q1 through Q4, C1, C2, CT1, D1 and D2, D3, T1, T2 and T3, and U6. Their design is standard. Also, design associated to current sensing and protection is also standard. This includes CT1, D1, D2, R5 and C5.

8.2.1.2.2 Step 2, Feedback Loop Design

D3 (TLV431) with U6, R6, R9, R10, R12, R13, C11 and C12 are composed of standard type 3 feedback loop compensation network and output voltage set point. Their design is also standard.

Table 2. Specifications for the Design Example

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	36	48	72	VDC
V_{OUT}	Output voltage		3.3		VDC
P_{OUT}	Output power			75	W
I_{OUT}	Output load current			23	A
C_{OUT}	Load capacitance			5000	µF
f_{SW}	Switching frequency		150		kHz
P_{LIMIT}	Over-power limit			150%	
η	Efficiency at full load		90%		
	Isolation	1500			V

8.2.1.2.3 Step 3, Programming the Device

8.2.1.2.3.1 Step 3-1

Equation 3 is used to determine RT based on switching frequency, 300 kHz and assumes the dead time of 150 ns.

$$R_T = \frac{\frac{1}{2 \times f_{SW}} - T_{d(SP)}}{33.2\,pF} = \frac{\frac{1}{2 \times 150\,kHz} - 150\,ns}{33.2\,pF} = 94.9\,k\Omega \Rightarrow R4 = 100\,k\Omega \quad (29)$$

8.2.1.2.3.2 Step 3-2, Determine RAMP Resistance and Capacitance

There are two-fold considerations to determine RAMP resistance and capacitance. Equation 23 provides RAMP consideration for SR initial start-up with prebias. The corresponding RAMP peak voltage is determined with input voltage low line and maximum prebias output voltage. In the following, T1 turns ratio n = 4.

$$V_{RAMP} = \frac{\frac{V_{IN}}{2 \times n} - V_{pre-bias}}{2 \times V_{pre-bias}} \times V_{SR\_RAMP} = \frac{\frac{36\,V}{2 \times 4} - 3.0\,V}{2 \times 3.0\,V} \times 3.0\,V = 0.750\,V \quad (30)$$

Equation 24 and Equation 25 provides RAMP consideration for soft start completion to make duty cycle match (1-D) = SR_D.

1. Calculate OUTA or OUTB duty cycle at 75-V input voltage, 3.3-V output.

$$D = \frac{n \times V_O}{\frac{V_{IN}}{2}} \times \frac{1}{2} = \frac{4 \times 3.3\,V}{75\,V/2} \times \frac{1}{2} = 0.176 \quad (31)$$

2. Calculate SRA or SRB duty cycle.

$$SR\_D = 1 - D = 1 - 0.176 = 0.82 \quad (32)$$

3. Calculate the COMP voltage value in steady state (Equation 24).

$$V_{COMP} = (SR\_D - 0.5) \times 3.0\,V \times 2 = (0.824 - 0.5) \times 3.0\,V \times 2 = 1.944\,V \quad (33)$$

4. Calculate the RAMP peak value (Equation 25).

$$V_{RAMP} = \frac{V_{COMP}}{(D \times 2)} = \frac{1.944\,V}{(0.176 \times 2)} = 5.523\,V \quad (34)$$

5. Arbitrary select C_{RAMP} 470 pF, then C3 = 470 pF.
6. Calculate R_{RAMP}.

$$R_{RAMP\_1} = \frac{1}{2 \times \ln\left(\frac{V_{CHARGE}}{V_{CHARGE} - V_{RAMP}}\right) \times C_{RAMP} \times f_{sw}} = \frac{1}{2 \times \ln\left(\frac{36\,V}{36\,V - 0.750\,V}\right) \times 470\,pF \times 150\,kHz} = 336.9\,k\Omega \quad (35)$$

$$R_{RAMP\_2} = \frac{1}{2 \times \ln\left(\frac{V_{CHARGE}}{V_{CHARGE} - V_{RAMP}}\right) \times C_{RAMP} \times f_{sw}} = \frac{1}{2 \times \ln\left(\frac{75\,V}{75\,V - 5.523\,V}\right) \times 470\,pF \times 150\,kHz} = 92.7\,k\Omega \quad (36)$$

As different RAMP resistor values are obtained, at this stage, we may take their average value for initial design.

8.2.1.2.4 Step 3-3, Determine Soft-Start Capacitance

Determine soft-start capacitance with soft-start time 15 ms.

$$C_{SS} = \frac{27\,\mu A \times T_{SS}}{V_{COMP(final)}} = \frac{27\,\mu A \times 15\,ms}{4.0\,V} = 0.101\,\mu F \Rightarrow C8 = 0.1\,\mu F \quad (37)$$

8.2.1.2.5 Step 3-4, Determine Dead-Time Resistance

Assuming the dead time is 150 ns, Select R7 = R8 = 121 kΩ based on Figure 27 and Figure 28.

8.2.1.2.6 Step 3-5, Determine OCP Hiccup Off-Time Capacitance

Assuming off time is 0.8 s (Equation 15).

$$C_{HICC} = T_{HICC} \times \frac{2.7\,\mu A}{2.4\,V - 0.3\,V} = 0.8\,s \times \frac{2.7\,\mu A}{2.4\,V - 0.3\,V} = 1.03\,\mu F \Rightarrow C7 = 1.0\,\mu F \quad (38)$$

8.2.1.2.7 Step 3-6, Determine Primary-Side OVP Resistance

Assuming OV_OFF = 73 V, OV_ON = 72 V (Equation 16 to Equation 18).

$$R_2 \le \frac{0.7\,V \times (V_r - V_f)}{11\,\mu A \times (V_r - 0.7\,V)} = \frac{0.7\,V \times (73\,V - 72\,V)}{11\,\mu A \times (73\,V - 0.7\,V)} = 880\,\Omega \Rightarrow R2 = 866\,\Omega \quad (39)$$

$$R_1 = \frac{V_R - 0.7\,V}{0.7\,V} \times R_2 = \frac{73\,V - 0.7\,V}{0.7\,V} \times 866\,\Omega = 89.4\,k\Omega \Rightarrow R1 = 88.7\,k\Omega \quad (40)$$

$$R_3 = \frac{0.7\,V \times (V_R - V_F) - 11\,\mu A \times R_2 \times (V_R - 0.7\,V)}{11\,\mu A \times V_r} =$$

$$= \frac{0.7\,V \times (73\,V - 72\,V) - 11\,\mu A \times 866\,\Omega \times (73\,V - 0.7\,V)}{11\,\mu A \times 73\,V} = 14\,\Omega \Rightarrow R14 = 14\,\Omega \quad (41)$$

8.2.1.2.8 Step 3-7, Select Capacitance for VDD and VREF

As recommended by the data sheet, select C6 = C4 = 1 µF. The final design is shown in Figure 46.

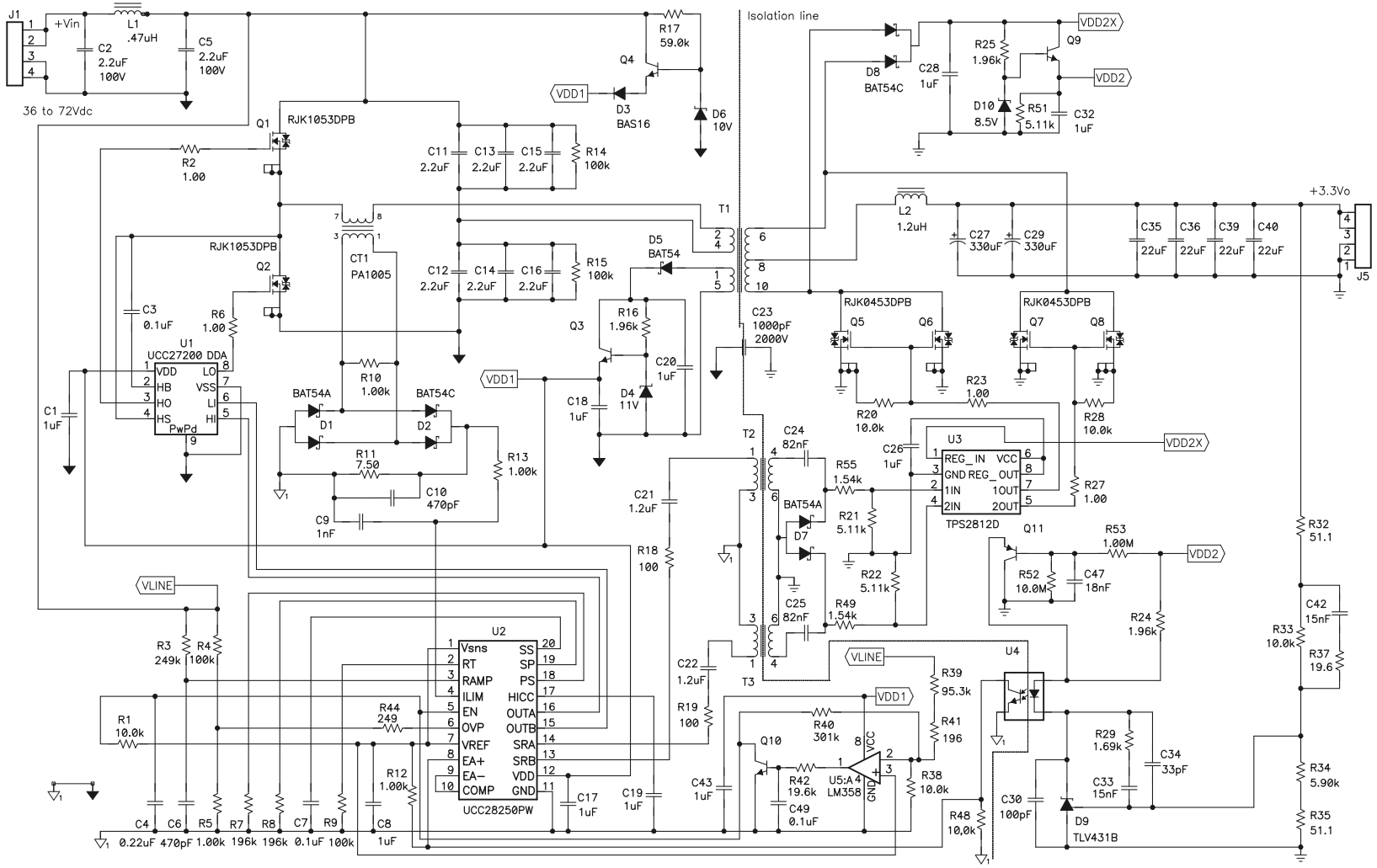


Figure 46. Schematics of Primary-Side Control Design Example

8.2.1.3 Application Curves

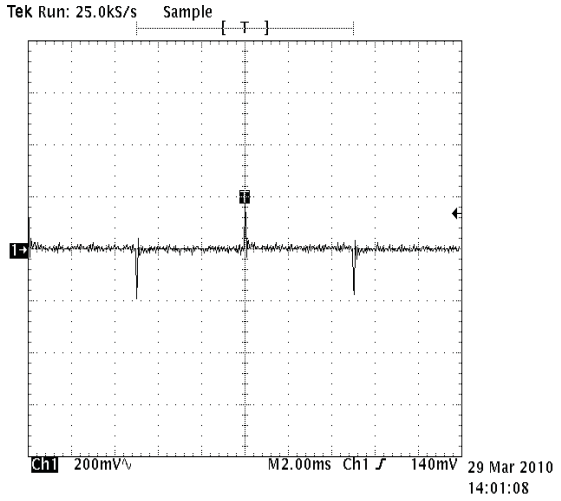


Figure 47. Load Transient

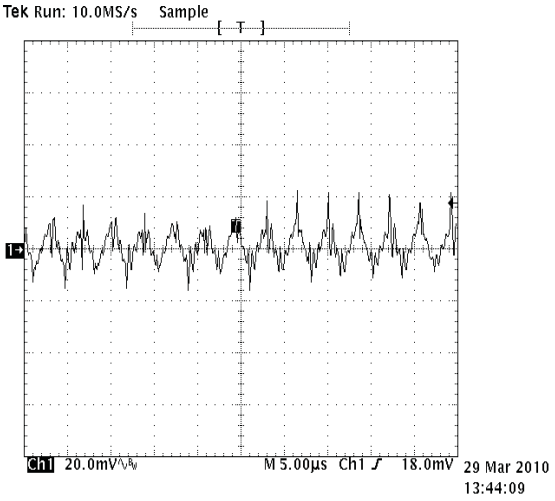


Figure 48. Output Ripple

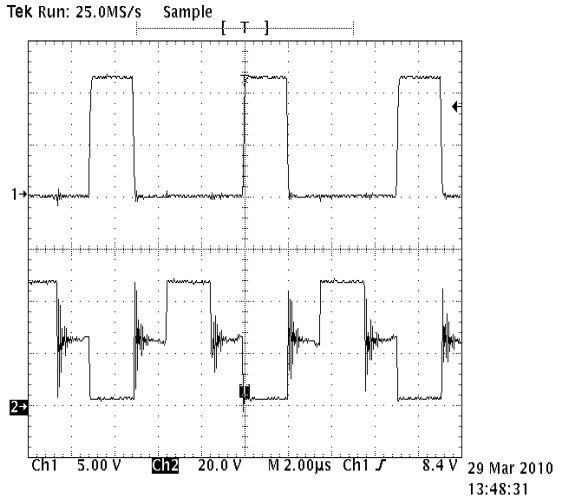


Figure 49. Clock Signal and Switching Node Waveform

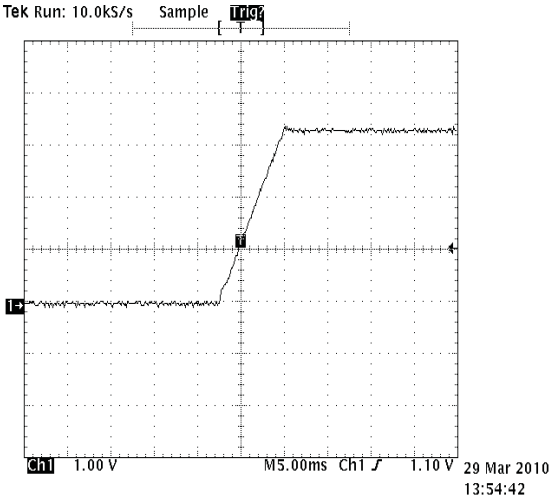


Figure 50. Enable Turnon Waveform

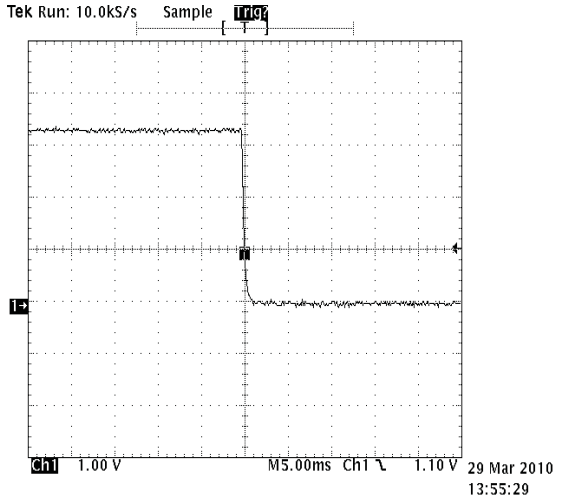


Figure 51. Enable Turnoff Waveform

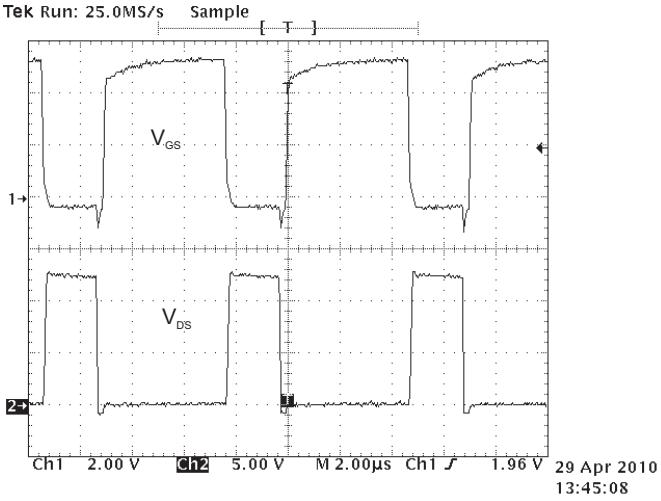


Figure 52. Secondary-Side Switching Waveform

8.2.2 Secondary-Side Half-Bridge Controller with Synchronous Rectification

UCC28250 also supports secondary-side control. Refer to Figure 53. In this configuration, the UCC28250 can be used in a design that produces smooth turnon performance with an output prebias condition. The design example and guidelines are summarized in *Designing UCC28250 as a Secondary Side Control for Output Turn-On with a Pre-Bias Condition*, SLAA477, and *Using the UCC28250EVM-564*, SLUU441.

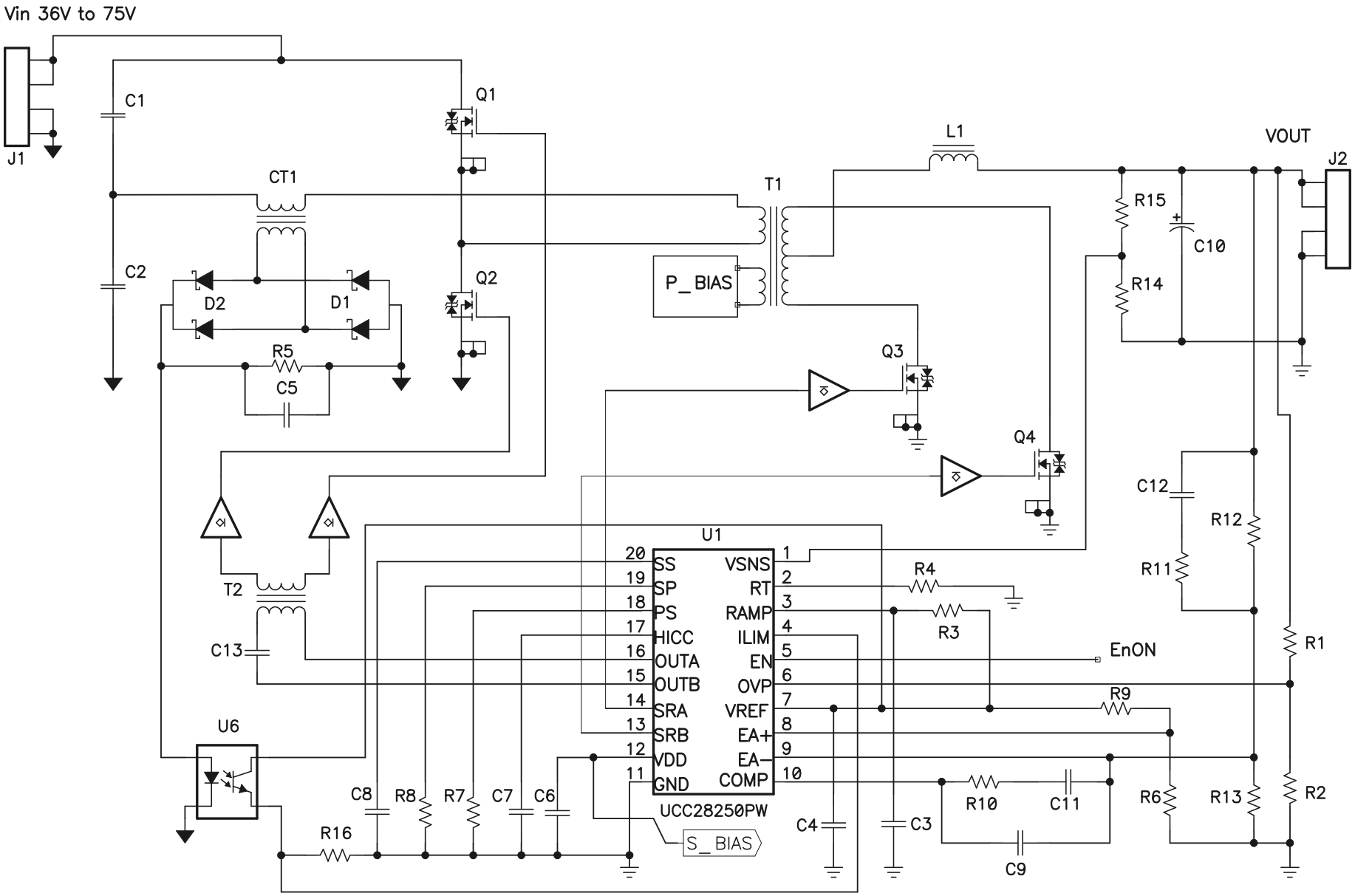


Figure 53. Secondary-Side Half-Bridge Controller With Synchronous Rectification

9 Power Supply Recommendations

The COMP pin is the internal error amplifier's output and also the input signal for PWM comparator. The maximum input common voltage of the PWM comparator is 2.8 V. TI suggests programming the peak value of RAMP to be lower than 2.3 V. Otherwise, the voltage of COMP pin should be clamp to be lower than 2.8 V by external circuit to make the internal PWM comparator work properly. Refer to *COMP (3/10)* for the detail information.

10 Layout

10.1 Layout Guidelines

To increase the reliability and robustness of the design, the following layout guidelines must be met.

1. REF/EA+ The REF/EA+ pin is the noninverting input of the error amplifier. For secondary side control, this pin is used to set the reference of voltage loop which decides the output voltage. So it is important to keep it clear from any of high voltage switching nodes. In addition, a decoupling capacitor located closely is recommended. For primary side control, this pin must be connected to opto-coupler. it is important minimize the loop area by running the EA+ signal and GND trace in parallel.
2. FB/EA- Minimize the loop between FB/EA- and COMP and keep it clear from any of high voltage switch nodes to avoid the noise injection into to the compensation loop.
3. COMP Minimize the loop between FB/EA- and COMP and keep it clear from any of high voltage switch nodes to avoid the noise injection into to the compensation loop.
4. GND As with all PWM controllers, the effectiveness of the filter capacitors on the signal pins depends upon the integrity of the ground return. Place all decoupling and filter capacitors as close as possible to the device pins with short traces. The AGND pin is used as the return connection for the low-power signaling and sensitive signal so it should be separated from the power stage ground to avoid ground bouncing.
5. VDD, VREF The VCC pin must be decoupled to GND by minimum 1-μF ceramic capacitors placed close to the pins.
6. SRA, SRB, OUTA, OUTB The SRA and SRB gate drive pins can be used to drive the inputs of gate driver or to directly drive the primary winding of a gate-drive transformer or the to directly drive the input of isolator. The tracks connected to these pins carry high dv/dt signals. Minimize noise pickup by routing them as far away as possible from tracks connected to sensitive signal including EA+, EA-, COMP, VSENSE, RT, RAMP/CS, ILIM, PS, SP.
7. HICC, SS, EN, OVP/OTP The connection track between the pin and external corresponding capacitor should be short.
8. PS, SP, RT, VSENSE, RAMP/CS, ILIM These pins are noise sensitive so allocate the related resistor as close as possible with the good ground connection.

10.2 Layout Example

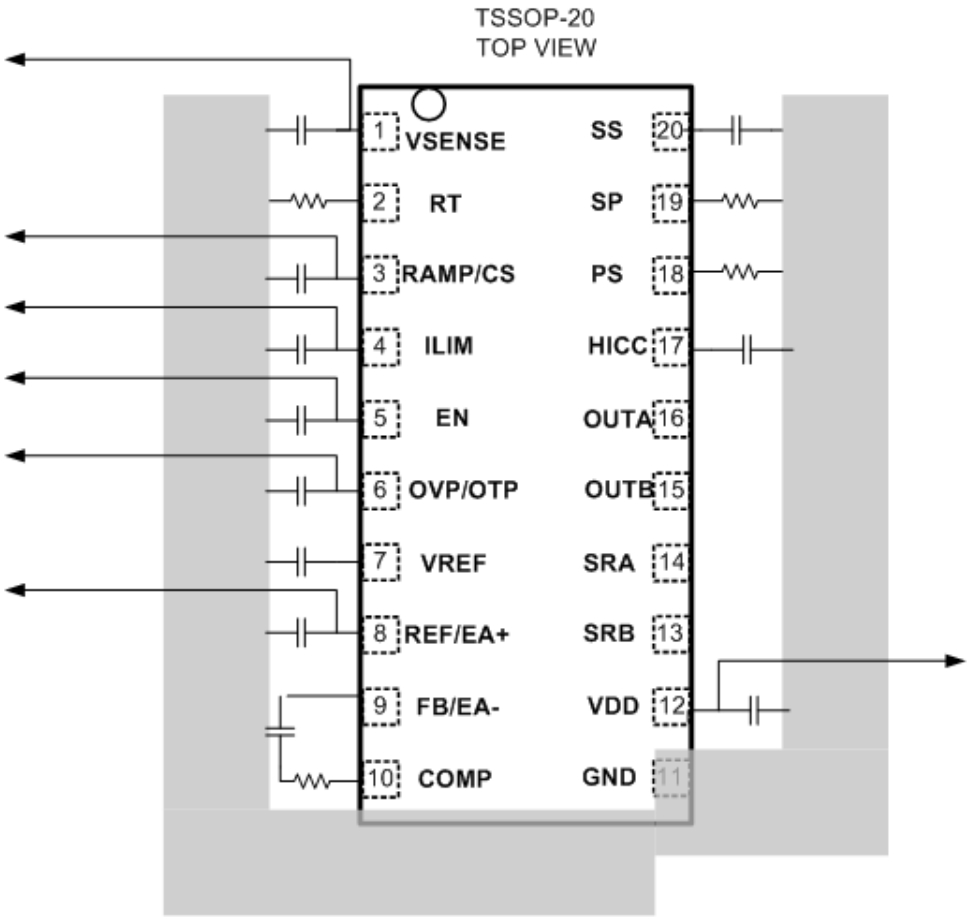


Figure 54. Layout Example

10.3 Thermal Protection

Internal thermal shutdown circuitry protects the UCC28250 in the event the maximum rated junction temperature is exceeded. When activated, typically at 160°C, with the maximum threshold at 170°C and minimum threshold at 150°C the controller is forced into a low power standby mode. The outputs (OUTA, OUTB, SRA, SRB) are disabled. This helps to prevent accidental device overheating. A 20°C hysteresis is added to prevent comparator oscillation. During thermal shutdown, the UCC28250 follows a normal start-up sequence after the junction temperature falls below 140°C (typical value, with 130°C minimum threshold and 150°C maximum threshold).

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Designing UCC28250 as a Secondary Side Control for Output Turn-On with a Pre-Bias Condition*, SLAA477
- *Using the UCC28250EVM-564*, SLUU441

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28250PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28250	Samples
UCC28250PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28250	Samples
UCC28250RGPR	ACTIVE	QFN	RGP	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	28250	Samples
UCC28250RGPT	ACTIVE	QFN	RGP	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	28250	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

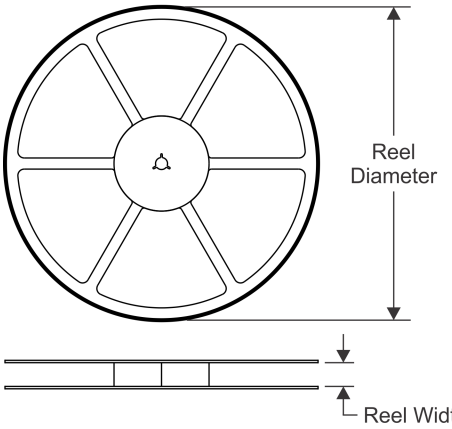
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

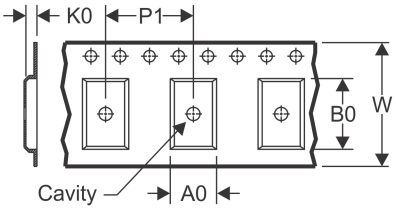
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

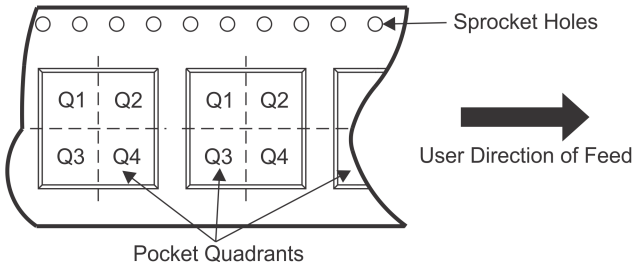


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

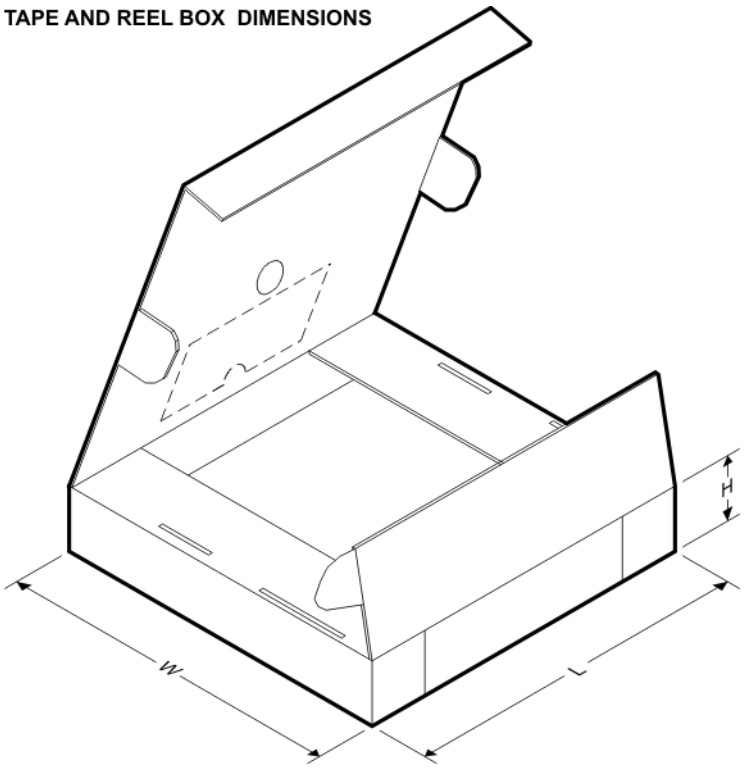
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28250PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
UCC28250RGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC28250RGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

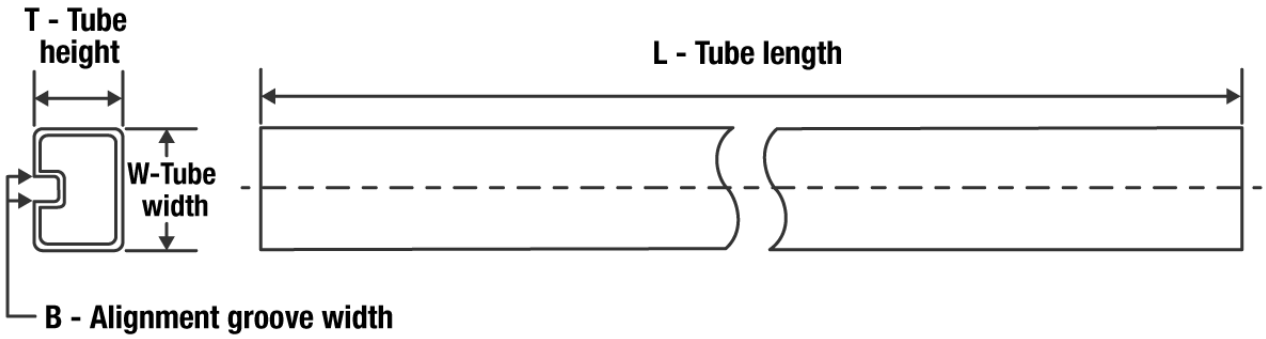
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28250PWR	TSSOP	PW	20	2000	853.0	449.0	35.0
UCC28250RGPR	QFN	RGP	20	3000	367.0	367.0	35.0
UCC28250RGPT	QFN	RGP	20	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

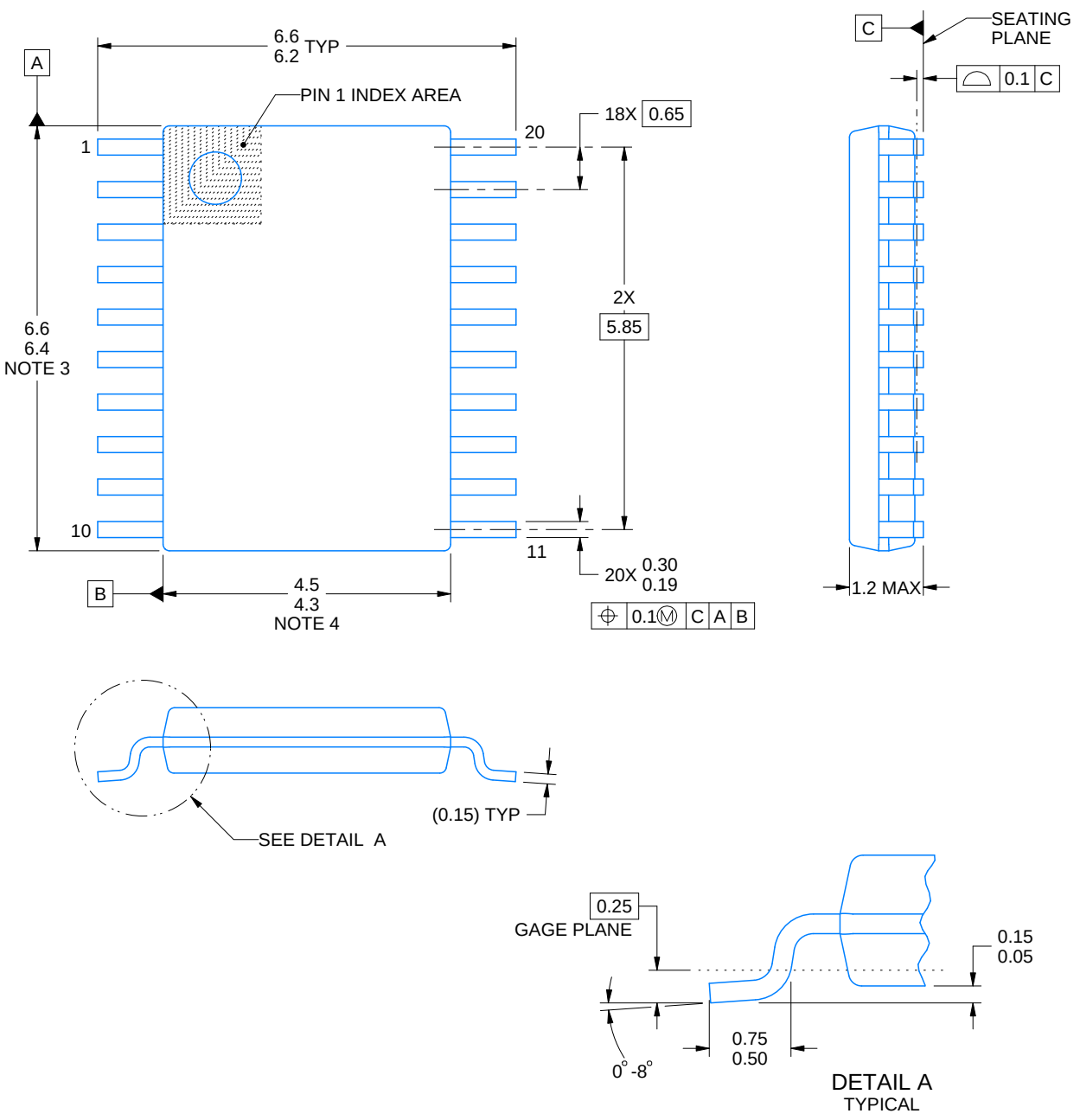
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC28250PW	PW	TSSOP	20	70	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0020A

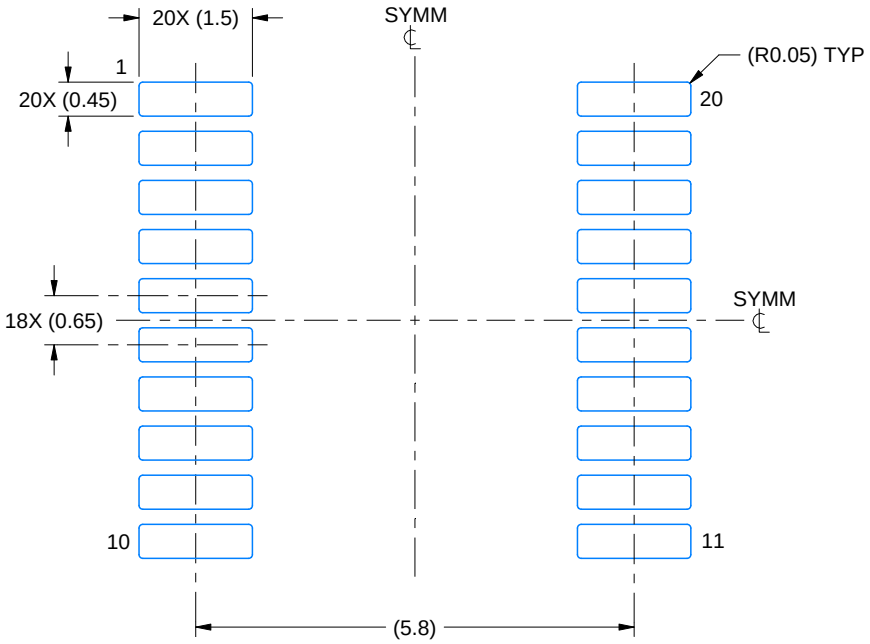
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



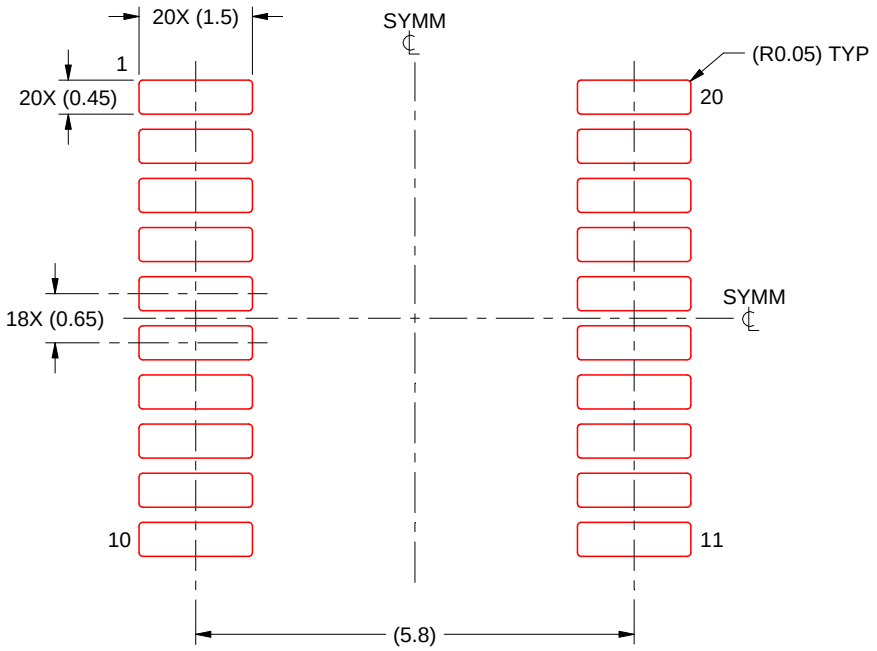
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



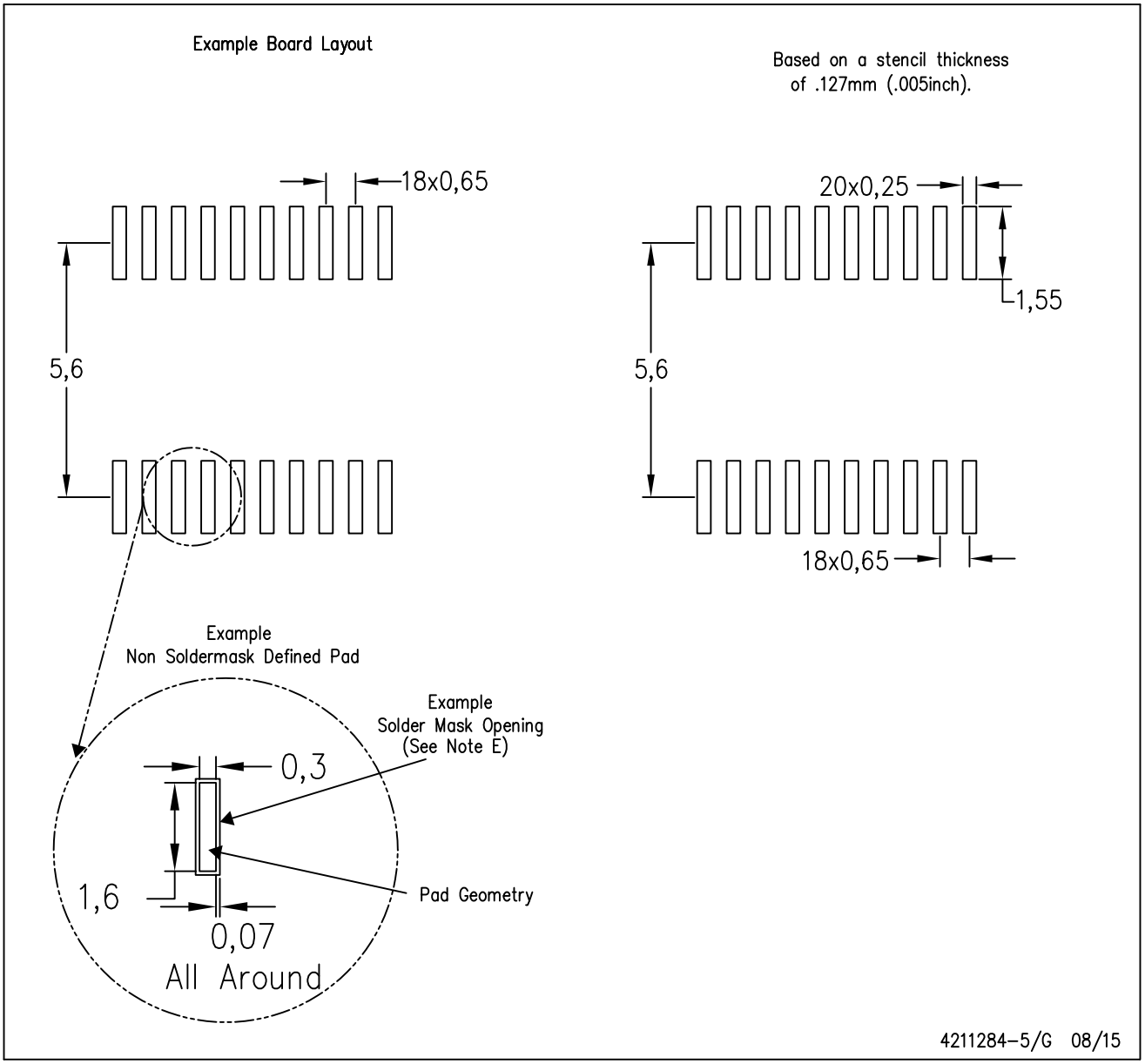
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

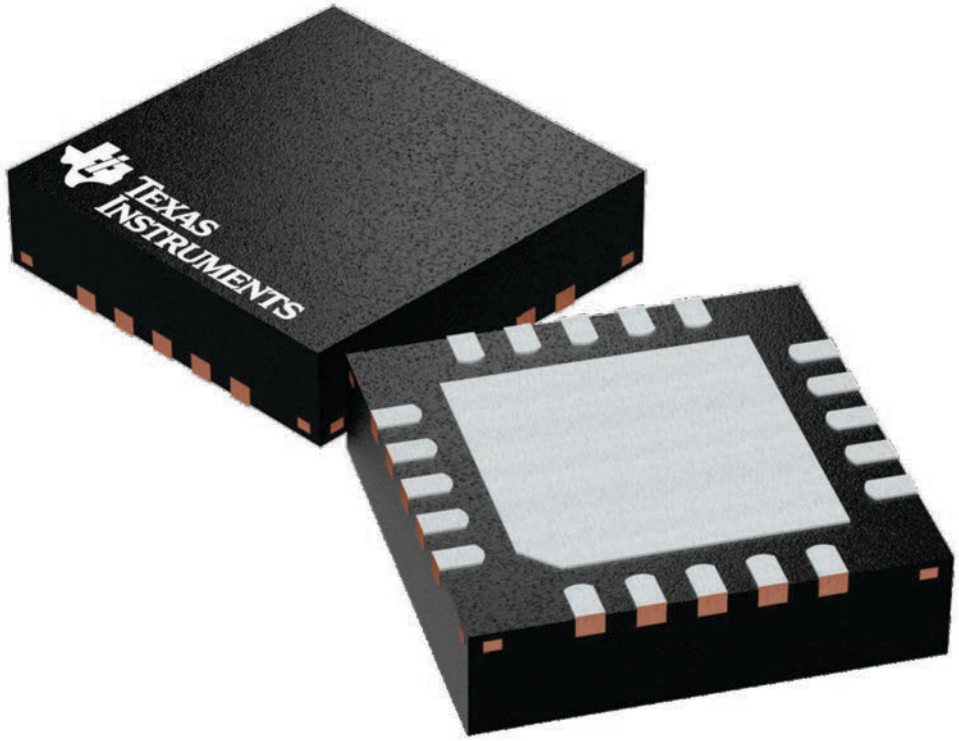
GENERIC PACKAGE VIEW

RGP 20

VQFN - 1 mm max height

4 x 4, 0.5 mm pitch

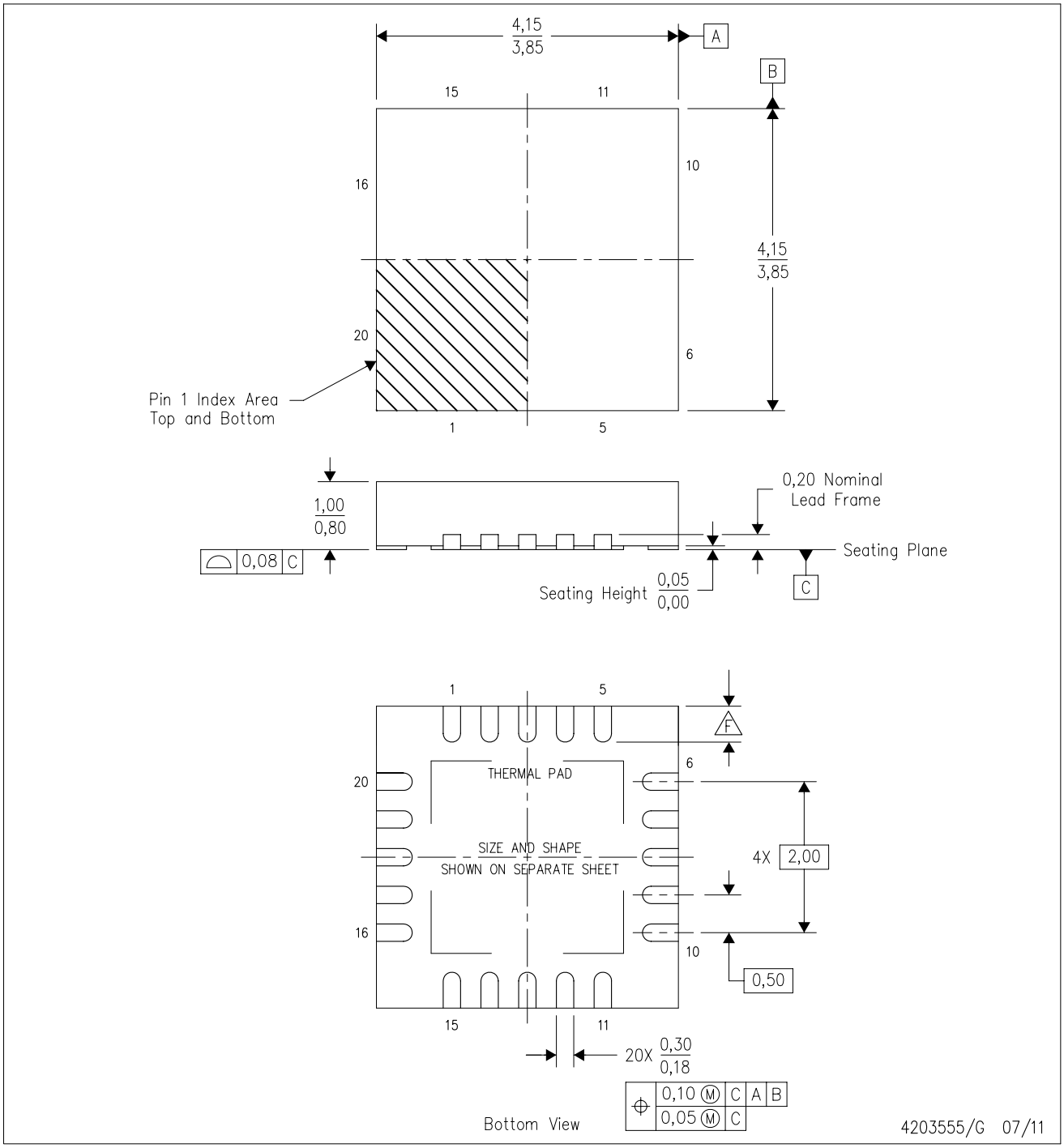
VERY THIN QUAD FLATPACK



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224735/A

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

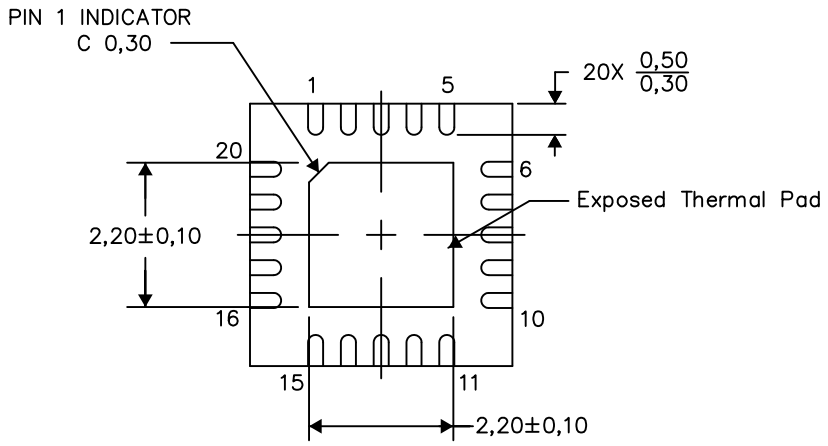
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



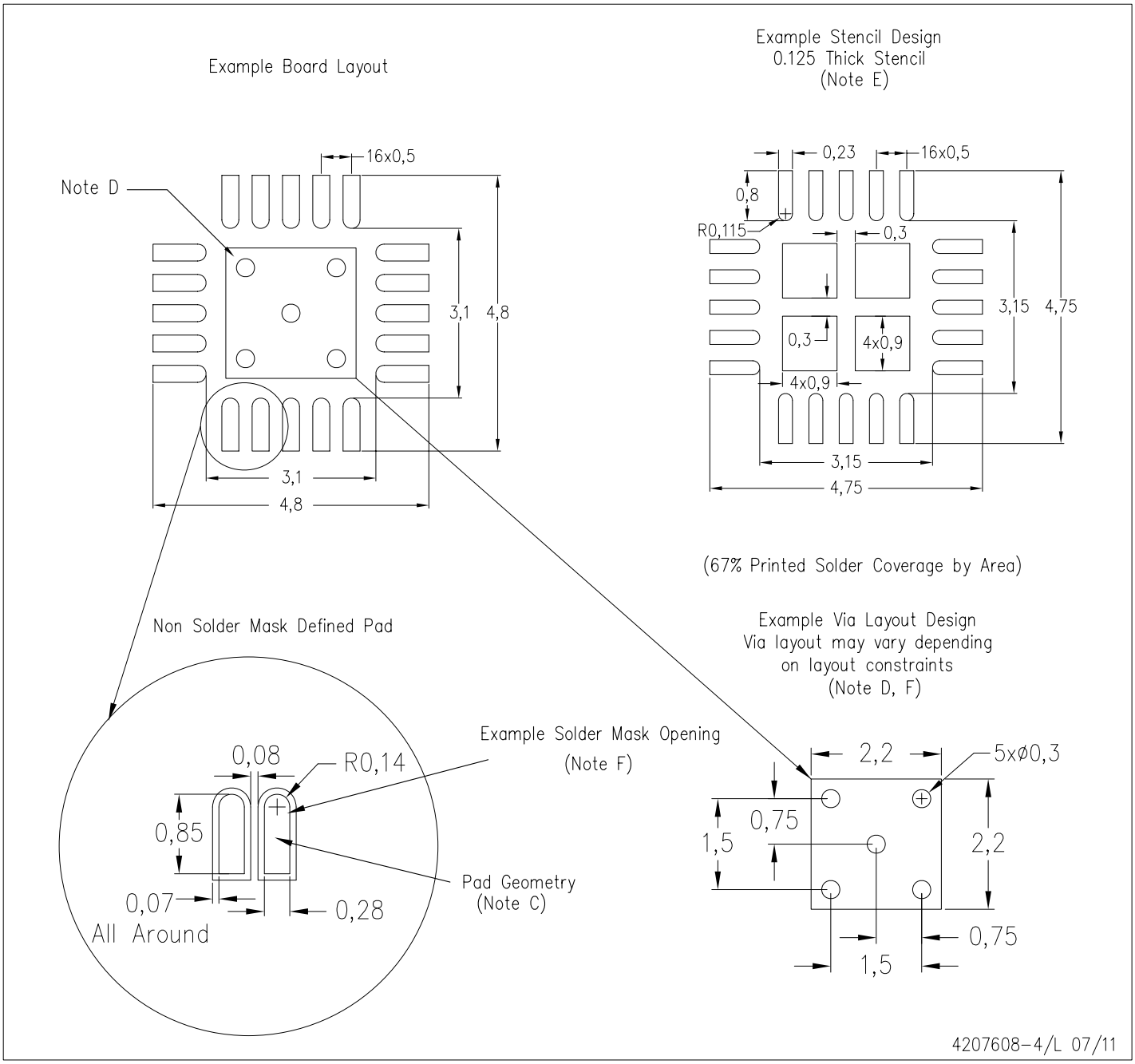
Bottom View

Exposed Thermal Pad Dimensions

4206346–4/AA 11/13

NOTES: A. All linear dimensions are in millimeters

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265