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# FDMS3016DC

## N-Channel Dual Cool™ 56 PowerTrench® MOSFET 30 V, 49 A, 6.0 mΩ



### Features

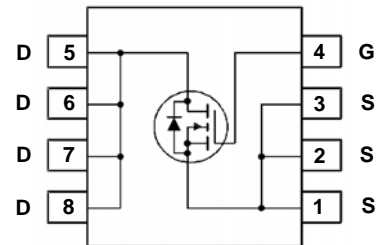
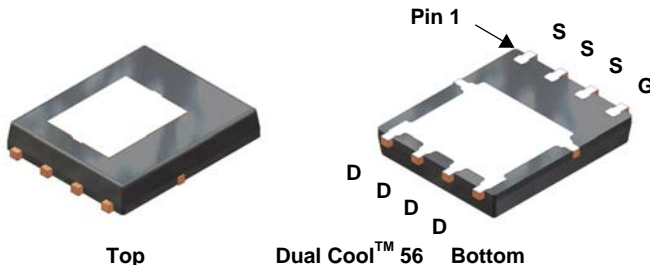
- Dual Cool™ Top Side Cooling PQFN package
- Max  $r_{DS(on)}$  = 6.0 mΩ at  $V_{GS}$  = 10 V,  $I_D$  = 12 A
- Max  $r_{DS(on)}$  = 9.0 mΩ at  $V_{GS}$  = 4.5 V,  $I_D$  = 10 A
- High performance technology for extremely low  $r_{DS(on)}$
- RoHS Compliant

### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process. Advancements in both silicon and Dual Cool™ package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

### Applications

- Synchronous Rectifier for DC/DC Converters
- Telecom Secondary Side Rectification
- High End Server/Workstation



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$	49	A
	-Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	78	
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	18	
	-Pulsed	200	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	72	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 4)	1.3	V/ns
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	60	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	3.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	5.7	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	2.1	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	11	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
3016	FDMS3016DC	Dual Cool™ 56	13"	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		17		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	1.0	1.9	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 12\text{ A}$		5.0	6.0	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 10\text{ A}$		7.0	9.0	
		$V_{GS} = 10\text{ V}$ , $I_D = 12\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		7.5	9.4	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 12\text{ A}$		44		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		1038	1385	pF
$C_{oss}$	Output Capacitance			513	685	pF
$C_{rss}$	Reverse Transfer Capacitance			87	135	pF
$R_g$	Gate Resistance			0.9		$\Omega$

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 12\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		9	18	ns	
$t_r$	Rise Time			3	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			19	35	ns	
$t_f$	Fall Time			2	10	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		16	23	nC
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to }4.5\text{ V}$	$V_{DD} = 15\text{ V}$ , $I_D = 12\text{ A}$	7.6	10.6	nC
$Q_{gs}$	Gate to Source Gate Charge		3			nC	
$Q_{gd}$	Gate to Drain "Miller" Charge		2.5			nC	

**Drain-Source Diode Characteristics**

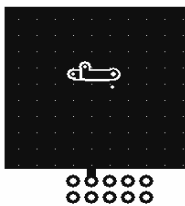
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 12\text{ A}$ (Note 2)		0.82	1.3	V
		$V_{GS} = 0\text{ V}$ , $I_S = 1.9\text{ A}$ (Note 2)		0.73	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 12\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		25	45	ns
$Q_{rr}$	Reverse Recovery Charge			9	18	nC

## Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	5.7	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	2.1	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1c)	27	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1e)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1f)	19	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1h)	61	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	11	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1l)	13	

### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 38  $^{\circ}\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 81  $^{\circ}\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

- c. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- d. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- e. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- f. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- g. 200FPM Airflow, No Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- h. 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- i. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- j. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- k. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- l. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3.  $E_{AS}$  of 72 mJ is based on starting  $T_J = 25^{\circ}\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = 12\text{ A}$ ,  $V_{DD} = 27\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

4.  $I_{SD} \leq 12\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^{\circ}\text{C}$ .

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

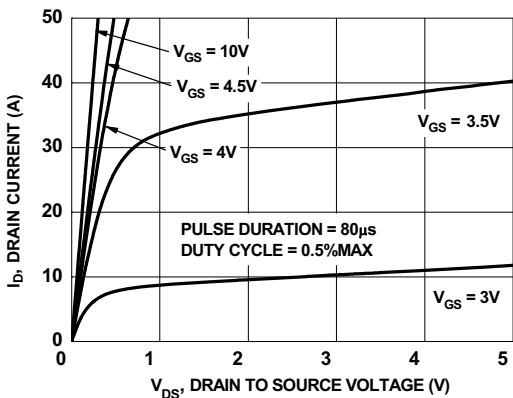


Figure 1. On-Region Characteristics

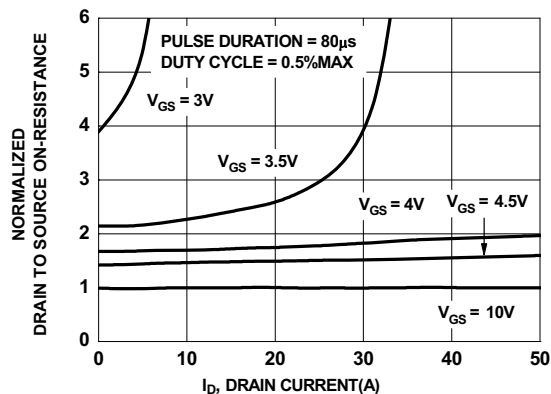


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

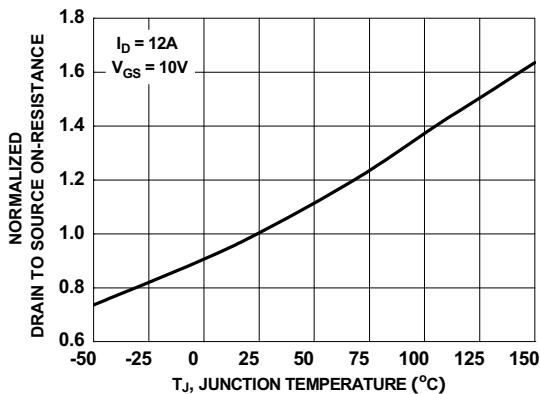


Figure 3. Normalized On-Resistance vs Junction Temperature

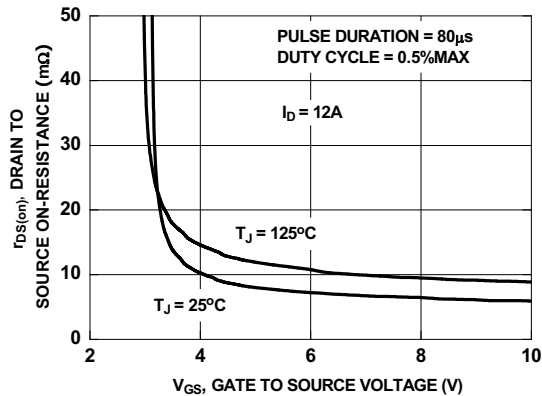


Figure 4. On-Resistance vs Gate to Source Voltage

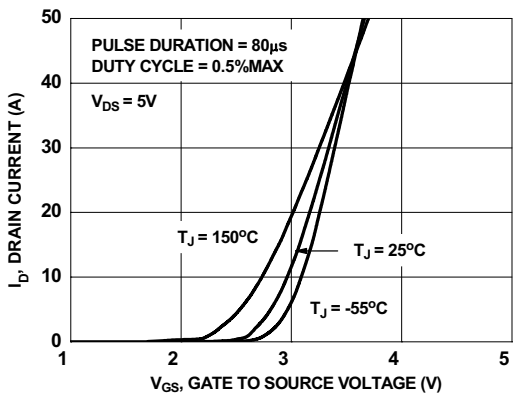


Figure 5. Transfer Characteristics

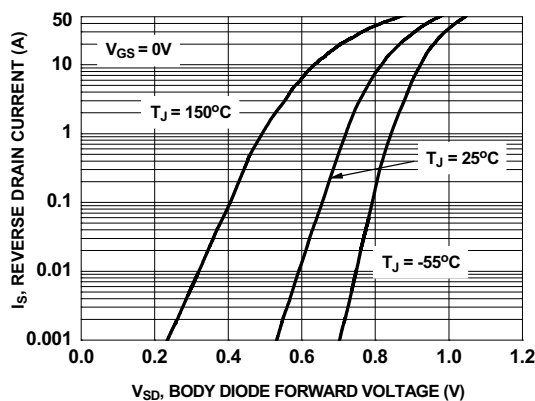
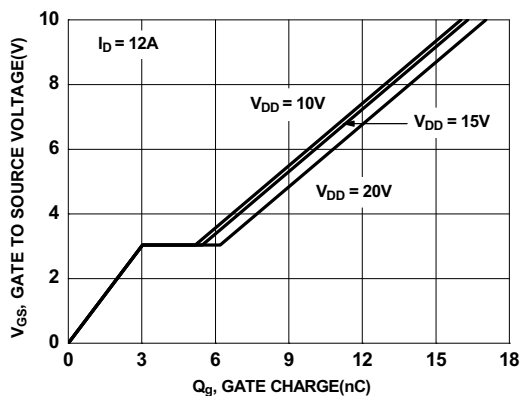
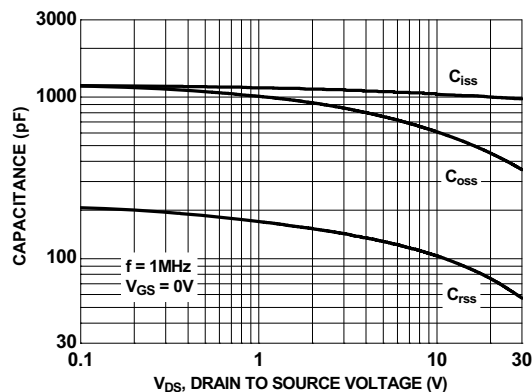


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

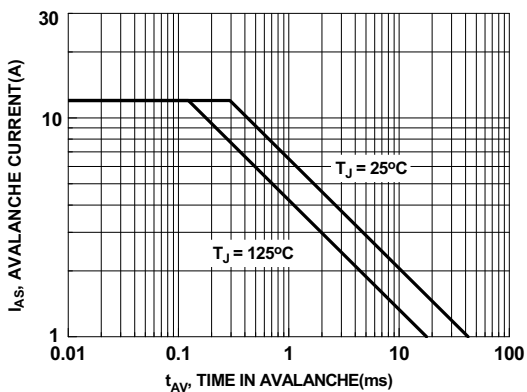
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



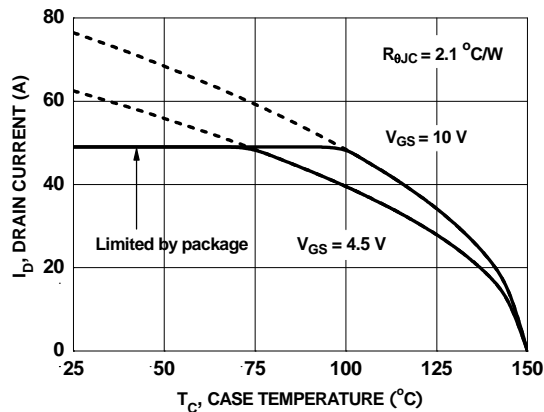
**Figure 7. Gate Charge Characteristics**



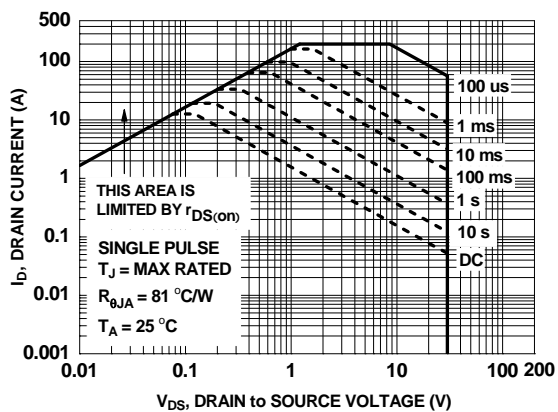
**Figure 8. Capacitance vs Drain to Source Voltage**



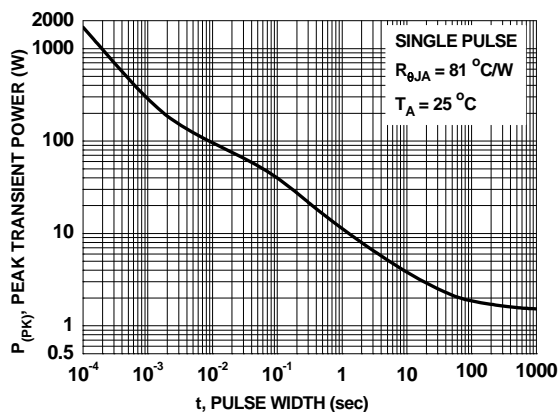
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

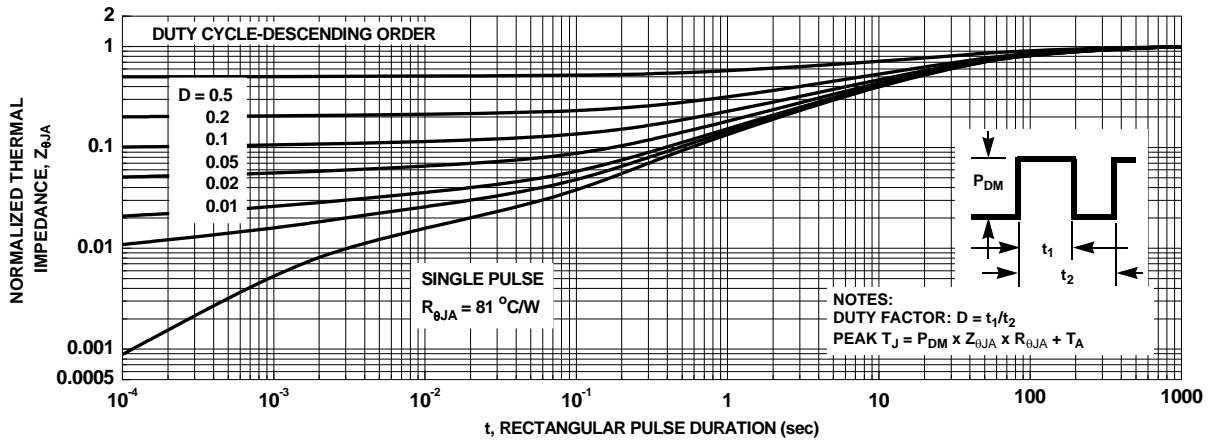


**Figure 11. Forward Bias Safe Operating Area**

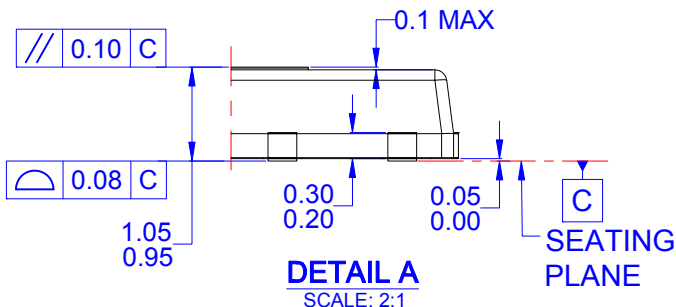
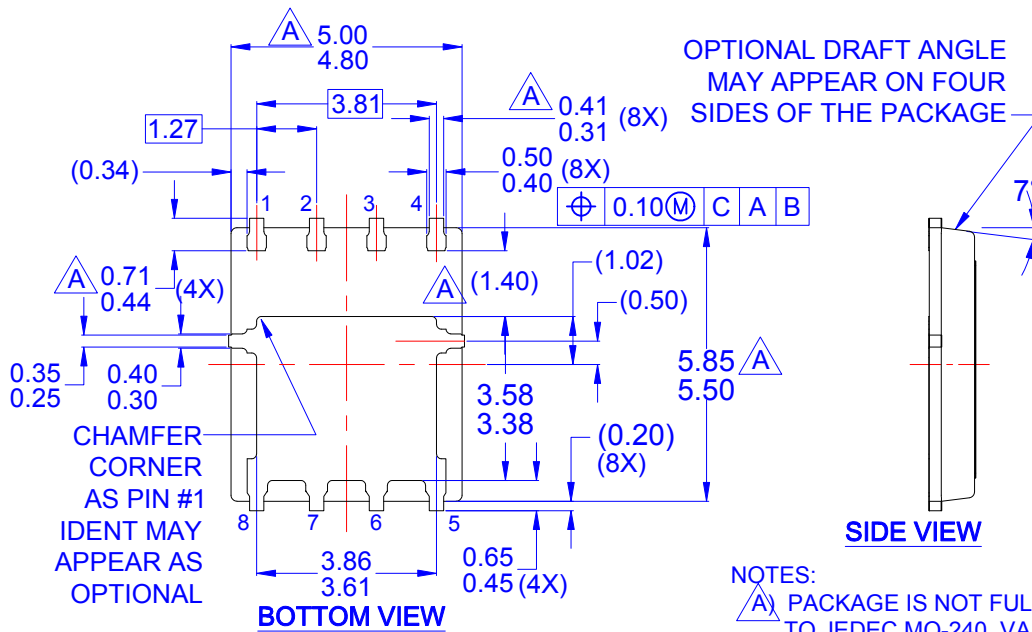
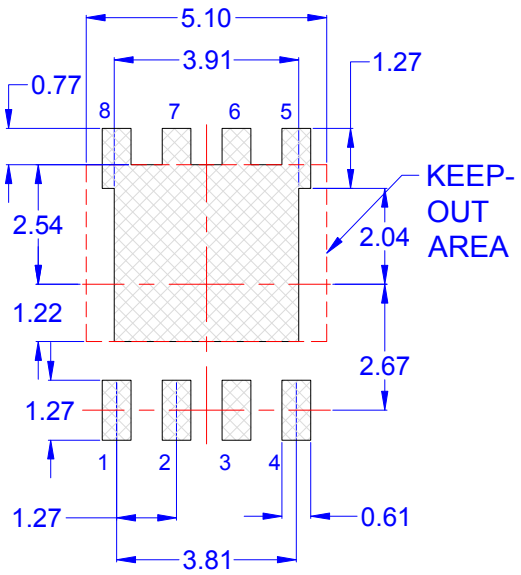
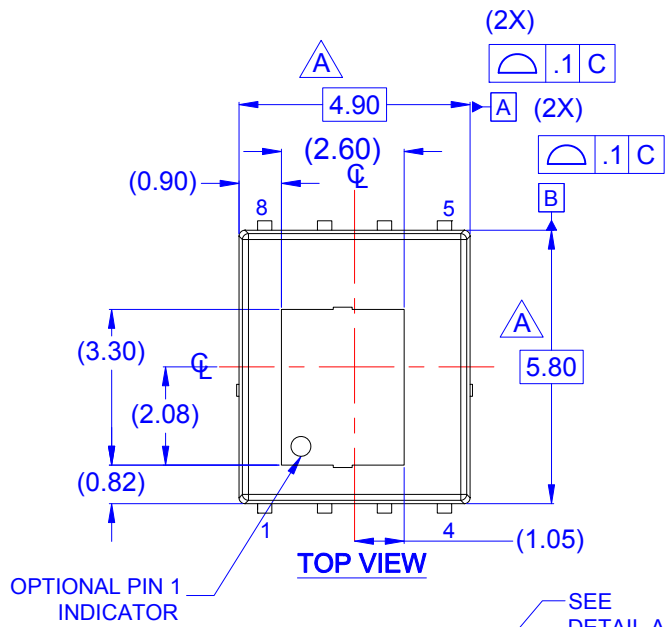


**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**



- NOTES:
- A) PACKAGE IS NOT FULLY COMPLIANT TO JEDEC MO-240, VARIATION AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
  - E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
  - F) DRAWING FILE NAME: PQFN08DREV4





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