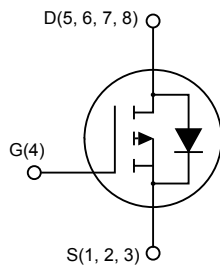
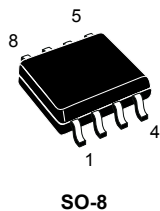


P-channel -30 V, 10 mΩ typ., -12.5 A, STripFET H6 Power MOSFET in an SO-8 package



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STS10P3LLH6	-30 V	12 mΩ	-12.5 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.



Product status link

[STS10P3LLH6](#)

Product summary

Order code	STS10P3LLH6
Marking	10K3L
Package	SO-8
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	-30	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	-12.5	A
	Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$	-7.8	
$I_{DM}^{(1)}$	Drain current (pulsed)	-50	A
P_{TOT}	Total power dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	2.7	W
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = -5\text{ A}$)	70	mJ
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		

1. Pulse width limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb	47	$^\circ\text{C/W}$

1. When mounted on 1 inch² FR-4 board, 2 oz. Cu., $t \leq 10\text{ s}$.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = -250\ \mu\text{A}$	-30			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\ \text{V}, V_{DS} = -30\ \text{V}$			-1	μA
		$V_{GS} = 0\ \text{V}, V_{DS} = -30\ \text{V}, T_C = 125\text{ °C}^{(1)}$			-10	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			-100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1.0	-1.7	-2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = -10\ \text{V}, I_D = -5\ \text{A}$		10	12	m Ω
		$V_{GS} = -4.5\ \text{V}, I_D = -5\ \text{A}$		14	17	

1. Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = -25\ \text{V}, f = 1\ \text{MHz}, V_{GS} = 0\ \text{V}$	-	3350	-	pF
C_{oss}	Output capacitance		-	414	-	pF
C_{rss}	Reverse transfer capacitance		-	287	-	pF
Q_g	Total gate charge	$V_{DD} = -15\ \text{V}, I_D = -10\ \text{A}, V_{GS} = -4.5\ \text{V}$ (see Figure 13. Gate charge test circuit)	-	33	-	nC
Q_{gs}	Gate-source charge		-	14	-	nC
Q_{gd}	Gate-drain charge		-	11	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = -15\ \text{V}, I_D = -5\ \text{A},$ $R_G = 4.7\ \Omega, V_{GS} = -10\ \text{V}$	-	12.8	-	ns
t_r	Rise time		-	112	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 12. Switching times test circuit for resistive load)	-	61	-	ns
t_f	Fall time		-	45	-	ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = -5\text{ A}$, $V_{GS} = 0\text{ V}$	-		-1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = -5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	25.2		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = -24\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	17.4		nC
I_{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	-1.4		A

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

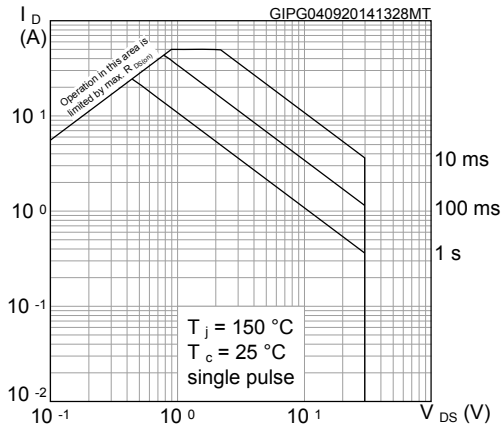


Figure 2. Thermal impedance

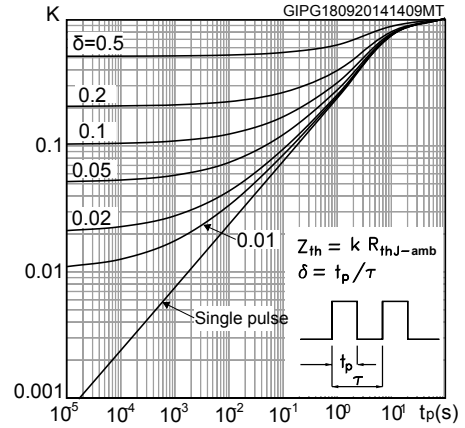


Figure 3. Output characteristics

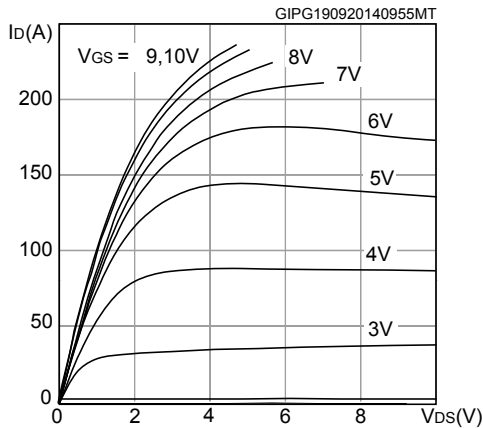


Figure 4. Transfer characteristics

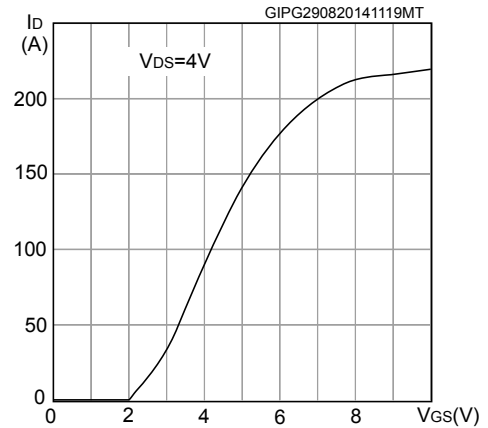


Figure 5. Gate charge vs gate-source voltage

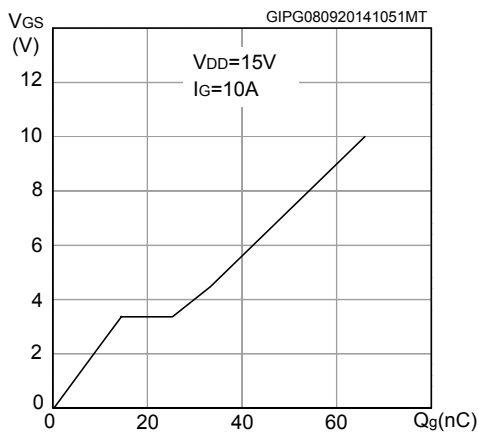


Figure 6. Static drain-source on-resistance

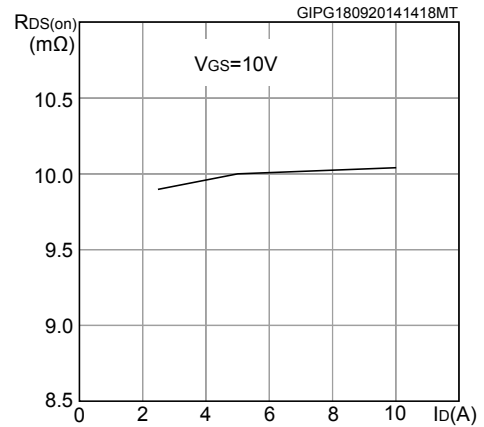


Figure 7. Capacitance variations

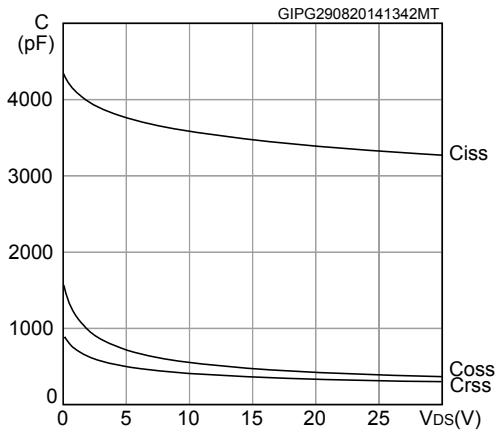


Figure 8. Normalized gate threshold voltage vs temperature

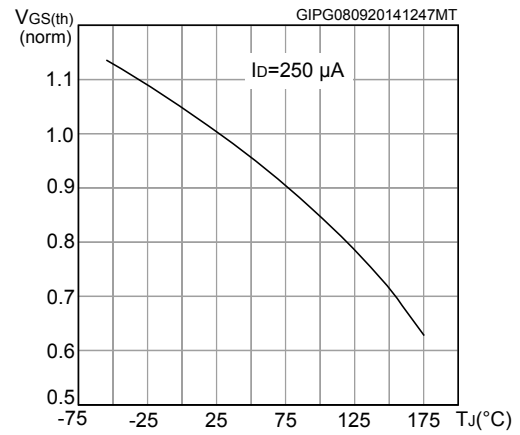


Figure 9. Normalized on-resistance vs temperature

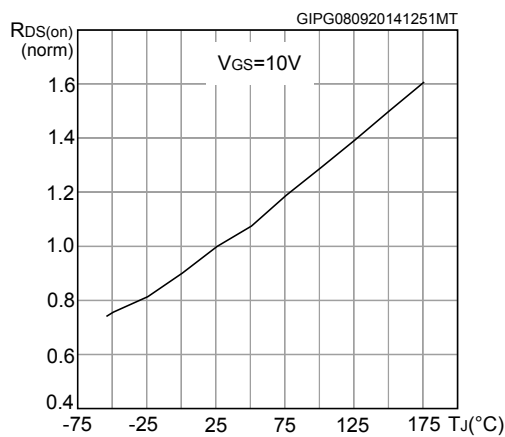


Figure 10. Normalized V(BR)DSS vs temperature

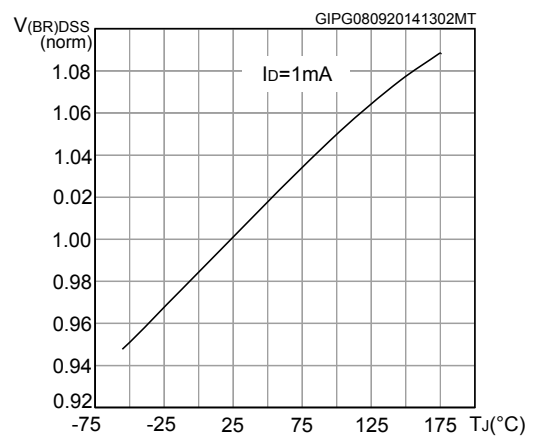
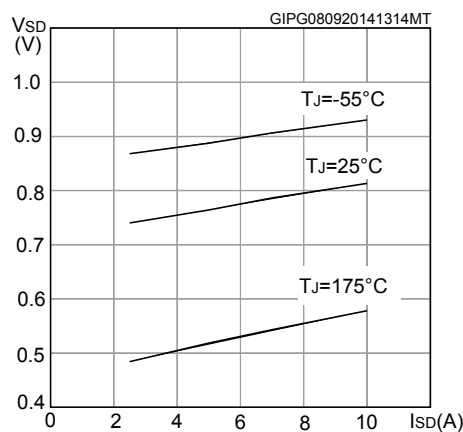


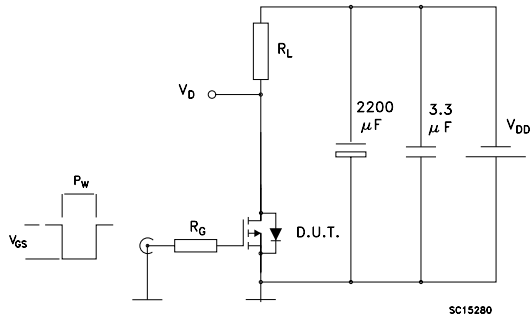
Figure 11. Source-drain diode forward characteristics



Note: For the P-channel Power MOSFET, current and voltage polarities are reversed.

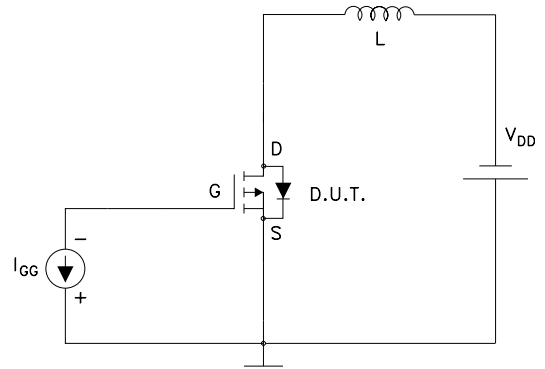
3 Test circuits

Figure 12. Switching times test circuit for resistive load



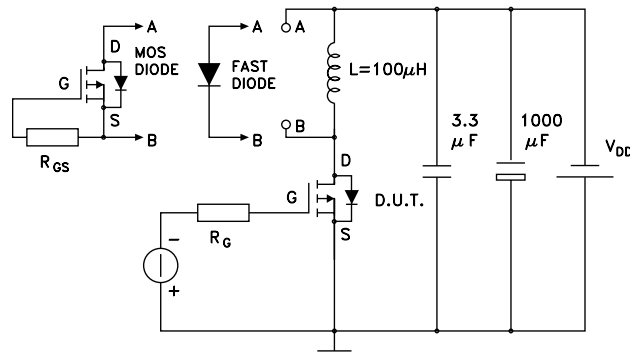
SC15280

Figure 13. Gate charge test circuit



SC15290

Figure 14. Test circuit for inductive load switching and diode recovery times



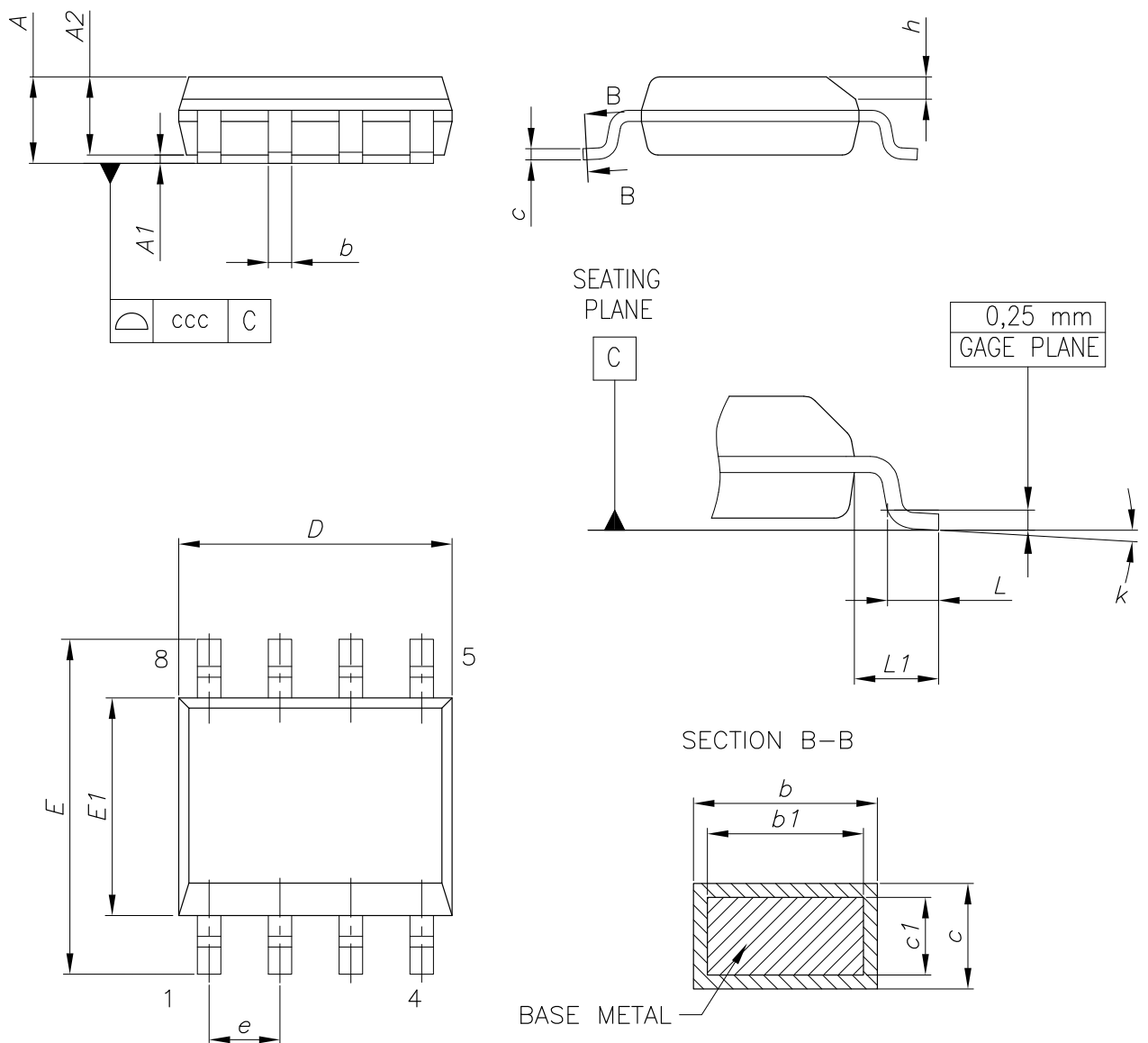
SC15300

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SO-8 package information

Figure 15. SO-8 package outline

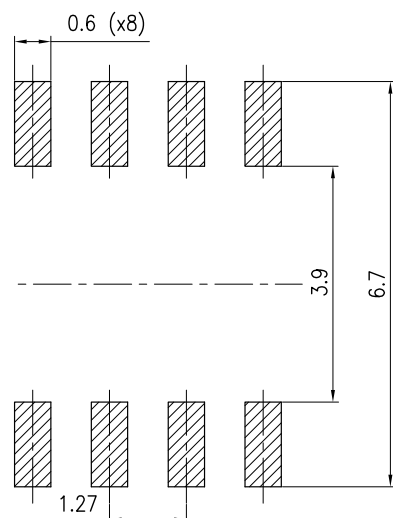


0016023_So-807_fig2_Rev10

Table 7. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

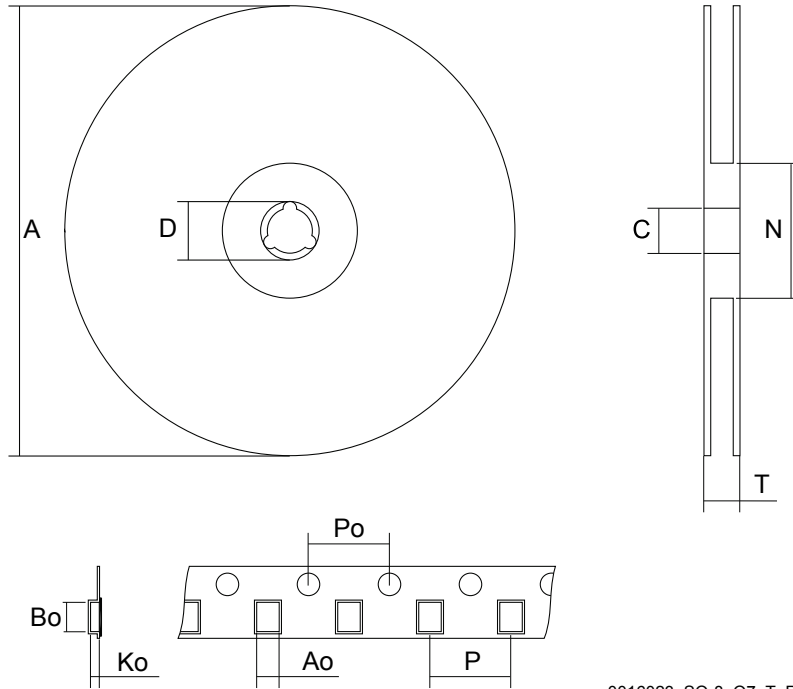
Figure 16. SO-8 recommended footprint (dimensions are in mm)



0016023_So-807_footprint_Rev10

4.2 SO-8 packing information

Figure 17. SO-8 tape and reel dimensions



0016023_SO-8_07_T_R

Table 8. SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	6.5	-	6.7
Bo	5.4		5.6
Ko	2.0		2.2
Po	3.9		4.1
P	7.9		8.1

Revision history

Table 9. Document revision history

Date	Revision	Changes
06-May-2014	1	Initial release.
24-Sep-2014	2	Updated the title, the features and the description in cover page. Updated Section 1: "Electrical ratings", Section 2: "Electrical characteristics". Added Section 2.1: "Electrical characteristics (curves)" Minor text changes.
11-Jun-2015	3	Text and formatting changes throughout document. On cover page: - updated title description and Features table In Section 1 Electrical ratings: - updated Table Absolute maximum ratings In section 2.1 Electrical characteristics (curves) - updated Figure Safe operating area Updated and renamed Section 4.1 SO-8 package information (was SO-8 mechanical data)
24-Aug-2015	4	Updated Table 4: "On/off states".
06-Dec-2016	5	Updated $V_{GS(th)}$ in Table 4: "On/off states". Minor text changes.
03-Apr-2017	6	Added E_{AS} value in <i>Table 2: "Absolute maximum ratings"</i> .
08-Jul-2020	7	Updated Internal schematic . Updated Section 4 Package information .

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3	Test circuits	7
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4.2	SO-8 packing information	10
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