CEL California Eastern Laboratories

Evaluation Board Document

NE5550779A-EV09-A

Evaluation Board

- Circuit Description
- Typical Performance Data
- Circuit Schematic and Assembly Drawing

Circuit Description

The NE5550779A-EV09-A is an evaluation circuit board for Renesas' LDMOS power FET, NE5550779A optimized for the performance at 915MHz. The circuit board is RoHS compliant.

Matching and Bias Circuits

Both input and output matching networks consist of shunt capacitors and sections of transmission lines (refer to the schematic and assembly drawing in the last page of this document for the component designation). The electrical lengths of the transmission lines labeled on the schematic are estimated and for reference only. Some bench tuning on the actual circuit board is usually required to achieve optimal performance. For applications where there is a constraint on the board space, serial inductors, instead of transmission lines, can be used for the matching circuits. The efficiency spec, PAE, usually will be slightly lower in that case.

LDMOSFETs essentially draw no gate current under normal operation conditions. Therefore a large value resistor, in the order of kΩ, can be used for the gate biasing. At the drain an inductor is used as the RF choke. The current rating for this inductor should be high enough to provide the required current at the operation conditions.

Bias Conditions

This evaluation board was optimized at a specific drain voltage, 7.5V. For different supply voltages, the matching circuits should be adjusted to fully utilize the device capability. The quiescent current is 100mA for the data shown below. The gain is higher at higher quiescent currents, particularly when the device is not completely saturated. For many communication systems, where the PA is never at idle state, a high quiescent current might be used.

PCB Material:

The PCB is Getek 28mil two layer board. The dielectric constant of Getek is 4.2.

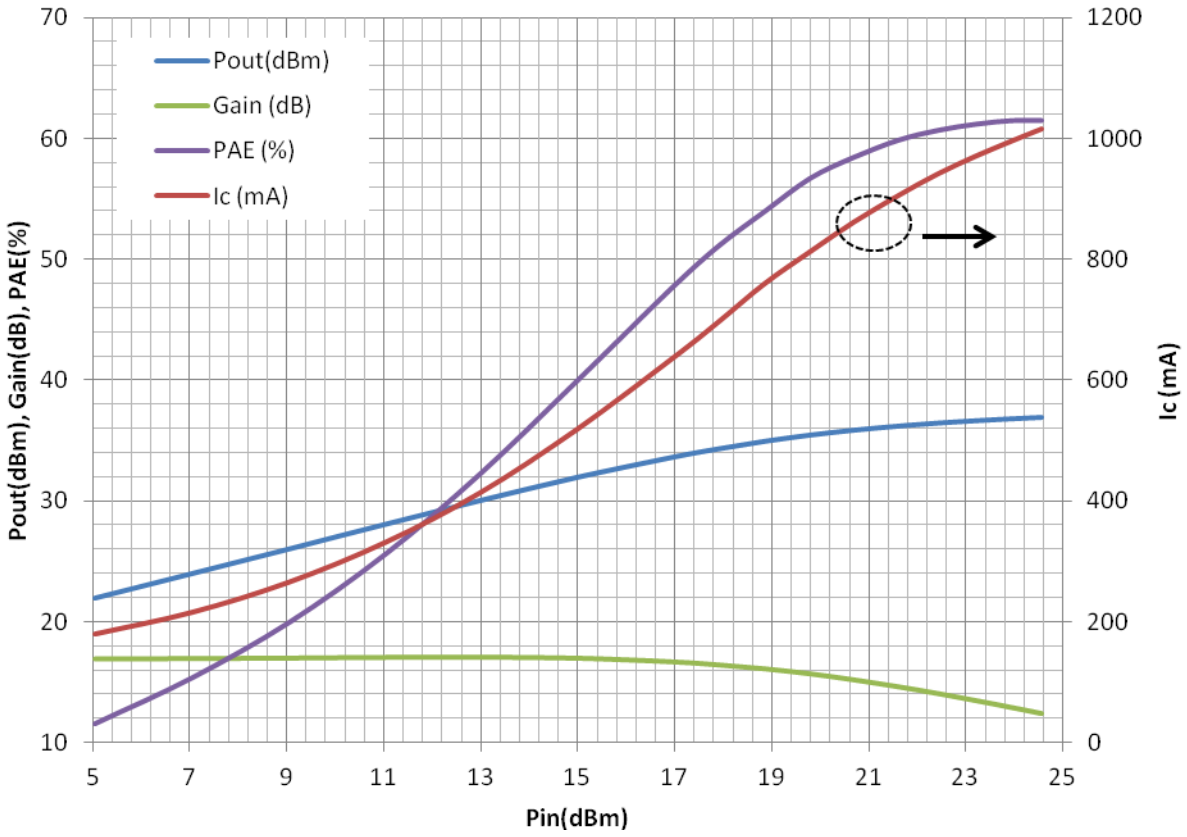
Typical Performance Data

Test Conditions:

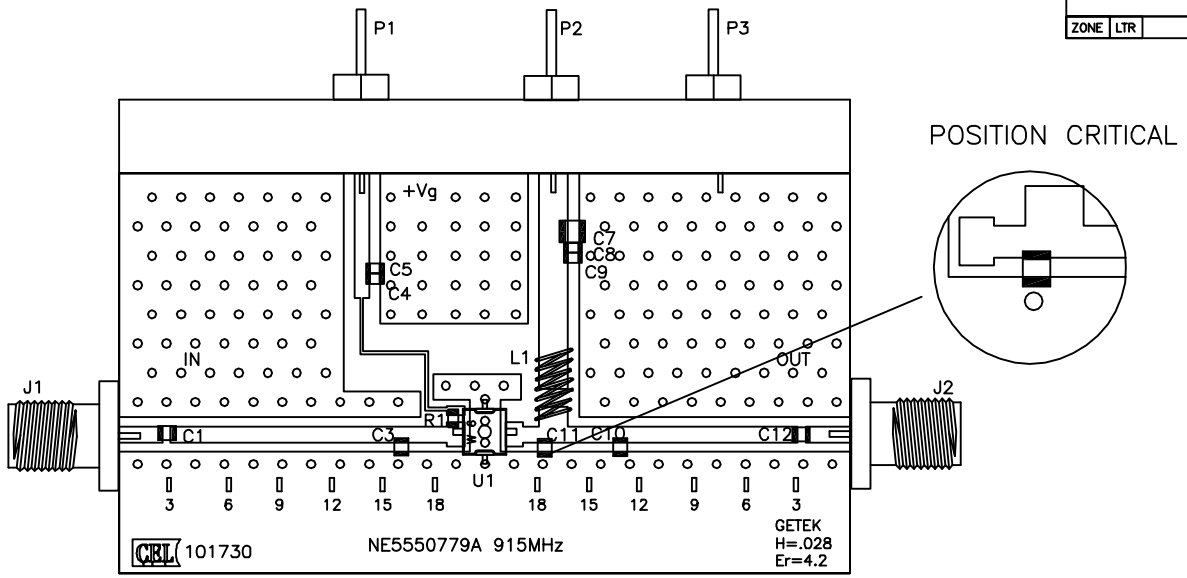
f=915MHz

Vd=7.5V, Idsq=100mA

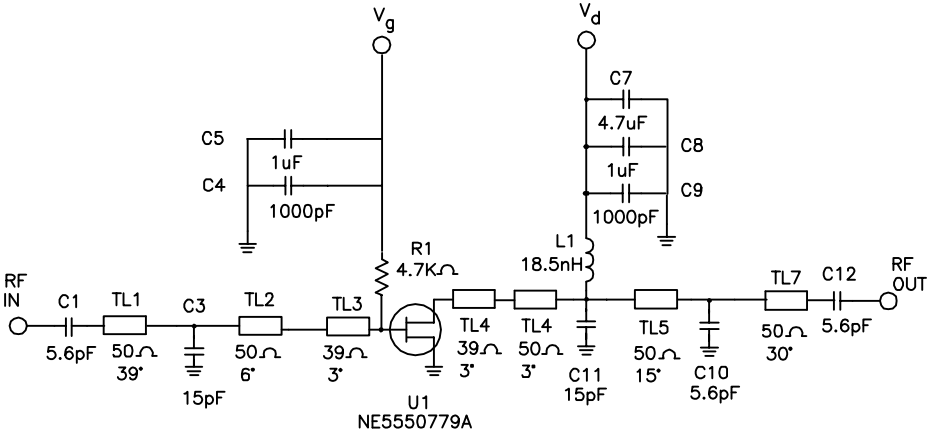
Pout, Gain, PAE and Current vs Pin are shown in the following plot.



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



POSITION CRITICAL



ITEM NO.	MATERIAL/SPECIFICATION	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	QTY
13	BLOCK		TF-101642	1
12	4.7uF 10V TANT CHIP CAP B MATS	C7	267M1002475K	1
11	0603 1000pF CAP MURATA	C4,C9	GRM1885C1H102JA01	2
10	0603 1uF CAP MURATA	C5,C8	GRM185R61C105KE44	2
9	5.6pF CAP ATC	C10	ATC100A220JT	1
8	15pF CAP ATC	C3,C11	ATC100A150JT	2
7	5.6pF CAP ATC	C1,C12	ATC100A6R8CT	2
6	0603 4.7 KOHM RES	R1	GENERIC	1
5	18.5nH 5 TURN INDUCTOR, COILCRAFT	L1	A05TJ	1
4	FEEDTHRU MURATA	P1, P2, P3	1205-003	3
3	SMA FEMALE CONNECTOR E.F.JOHNSON	J1, J2	142-0701-841	2
2	IC RENESAS	U1	NE5550779A	1
1	COMPONENT LAYOUT DRAWING	PCB	CL-101730	1

PARTS LIST

Note: All trace electrical lengths are at 915MHz

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS .XX± .01 .XXX± .005
ANGULAR ± 1°
DO NOT SCALE DRAWING
MATERIAL
FINISH

APPROVALS		
Drawing by:	M Dong	11/13/2012
Designed by:	M Dong	11/13/2012
Checked by:		
Project Engineer:		
Quality Control:		

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TITLE:
NE5550779A-EV09-A
915MHz

SIZE	FSCM NO.	DWG NO.	REV
C		AD102067	—

SCALE NONE	RELEASE DATE PROTOTYPE	SHEET 1 OF 1