LOW SKEW CLOCK INVERTER AND DIVIDER

ICS548A-03

Description

The ICS548A-03 is a low cost, low skew, high-performance general purpose clock designed to produce a set of one output clock, one inverted output clock, and one clock divided-by-two. Using our patented Phase-Locked Loop (PLL) techniques, the device operates from a frequency range of 10 MHz to 120 MHz in the PLL mode, and up to 160 MHz in the non-PLL mode.

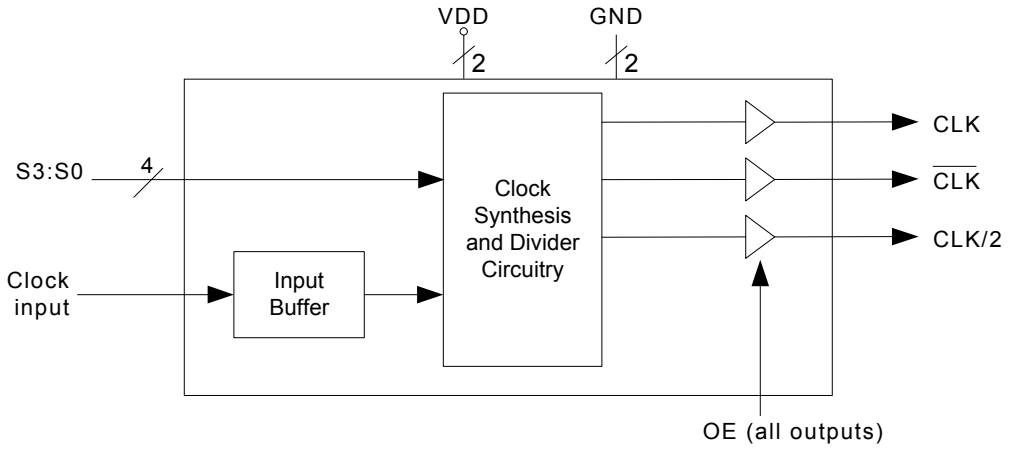
In applications that need to maintain low phase noise in the clock tree, the non-PLL (when S3=S2=1) modes should be used.

This chip is not a zero delay buffer. Many applications may be able to use the ICS527 for zero delay dividers.

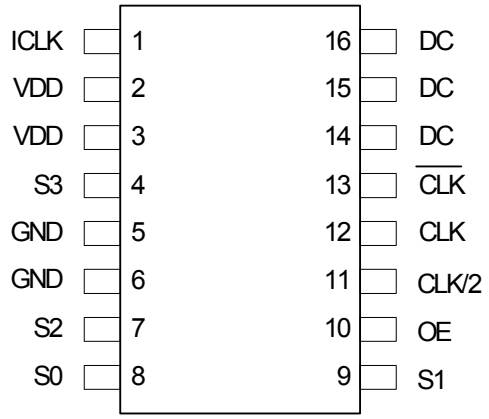
Features

- Packaged in 16-pin SOIC (150 mil)
- Input clock up to 160 MHz in the non-PLL mode
- Provides clock outputs of CLK, $\overline{CLK}$, and CLK/2
- Low skew (500 ps) on CLK, $\overline{CLK}$, and CLK/2
- All outputs can be tri-stated
- Entire chip can be powered down by changing one or two select pins
- 3.3 V operating range
- Available in commercial and industrial temperature ranges
- RoHS 5 (green) or RoHS 6 (green and lead free) compliant package

Block Diagram



Pin Assignment



CLK, $\overline{CLK}$, and CLK/2 Select Table (MHz)

S3	S2	S1	S0	CLK, $\overline{CLK}$	CLK/2	PLL	Input Range
0	0	0	0	Low	Low	OFF	Power Down
0	0	0	1	Input/4	Input/8	ON	30 - 120
0	0	1	0	Input	Input/2	ON	20 - 40
0	0	1	1	Input/2	Input/4	ON	20 - 80
0	1	0	0	Low	Low	OFF	Power Down
0	1	0	1	Input x 2	Input	ON	10 - 20
0	1	1	0	Input/5	Input/10	ON	40 - 120
0	1	1	1	Input/3	Input/6	ON	25 - 120
1	0	0	0	Low	Low	OFF	Power Down
1	0	0	1	Input/4	Input/8	ON	30 - 120
1	0	1	0	Input	Input/2	ON	20 - 40
1	0	1	1	Input/2	Input/4	ON	20 - 80
1	1	0	0	Low	Low	OFF	Power Down
1	1	0	1	Input/6	Input/12	OFF	0 - 160
1	1	1	0	Input/8	Input/16	OFF	0 - 160
1	1	1	1	Input/2	Input/4	OFF	0 - 80

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	ICLK	Input	Clock input.
2	VDD	Power	Connect to 3.3 V.
3	VDD	Power	Connect to 3.3 V.
4	S3	Input	Clock Select 3. See table on page 2.
5	GND	Power	Connect to ground.
6	GND	Power	Connect to ground.
7	S2	Input	Clock Select 2. See table on page 2.
8	S0	Input	Clock Select 0. See table on page 2.
9	S1	Input	Clock Select 1. See table on page 2.
10	OE	Input	Output Enable. Tri-states all clock outputs when low.
11	CLK/2	Output	Clock output divided by 2. See table on page 2.
12	CLK	Output	Clock output. See table on page 2.
13	$\overline{CLK}$	Output	Inverted clock output. See table on page 2.
14	DC	—	Don't connect. Do not connect anything to this pin.
15	DC	—	Don't connect. Do not connect anything to this pin.
16	DC	—	Don't connect. Do not connect anything to this pin.

External Components

The ICS548A-03 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01µF should be connected between pins 3 and 5, as close to the device as possible. Connect pin 2 directly to pin 3, and pin 6 directly to pin 5. A series termination resistor of 33Ω should be used on all clock outputs, as close to the device as possible. Leave any unused clock outputs floating. There are no pull-up resistors on the input pins, and they may be connected directly to VDD or ground.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS548A-03. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD (referenced to GND)	-0.5 V to 7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (commercial)	0 to +70° C
Ambient Operating Temperature (industrial)	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (commercial)	0		+70	° C
Ambient Operating Temperature (industrial)	-40		+85	° C
Power Supply Voltage (measured in respect to GND)	+3.13		+3.47	V

DC Electrical Characteristics

VDD = 3.3 V, Ambient temperature -40° C to +85° C , unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.13		3.47	V
Input High Voltage	V_{IH}	ICLK only (pin 1)	(VDD/2)+1	VDD/2		V
Input Low Voltage	V_{IL}	ICLK only (pin 1)		VDD/2	(VDD/2)-1	V
Input High Voltage	V_{IH}	All other inputs	2			V
Input Low Voltage	V_{IL}	All other inputs			0.8	V
Output High Voltage, CMOS level	V_{OH}	I_{OH} = -8 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Operating Supply Current, 100 MHz clock	IDD	S3=S2=S0=0, S1=1		20		mA
Short Circuit Current	I_{OS}	Each output		±50		mA
Input Capacitance	C_{IN}	All inputs		5		pF

AC Electrical Characteristics

VDD = 3.3 V, Ambient Temperature -40 to +85° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency, clock input, PLL on	f_{IN}		10		120	MHz
Input Frequency, clock input, PLL off	f_{IN}		0		160	MHz
Output Frequency (see table on page 2)	f_{OUT}	Mode dependent	0		120	MHz
Output Clock Rise Time	t_{OR}	0.8 to 2.0 V		0.84		ns
Output Clock Fall Time	t_{OF}	2.0 to 0.8 V		0.74		ns
Output Clock Duty Cycle	t_{DC}	At VDD/2	45	50	55	%
Output Enable Time, OE high to output on					50	ns
Output Disable Time, OE to tri-state					50	ns
Absolute Clock Period Jitter. PLL modes		Deviation from mean		150		ps
One Sigma Clock Period Jitter, PLL modes				60		ps
Output clock skew for CLK, $\overline{CLK}$, or CLK/2		At VDD/2			850	ps

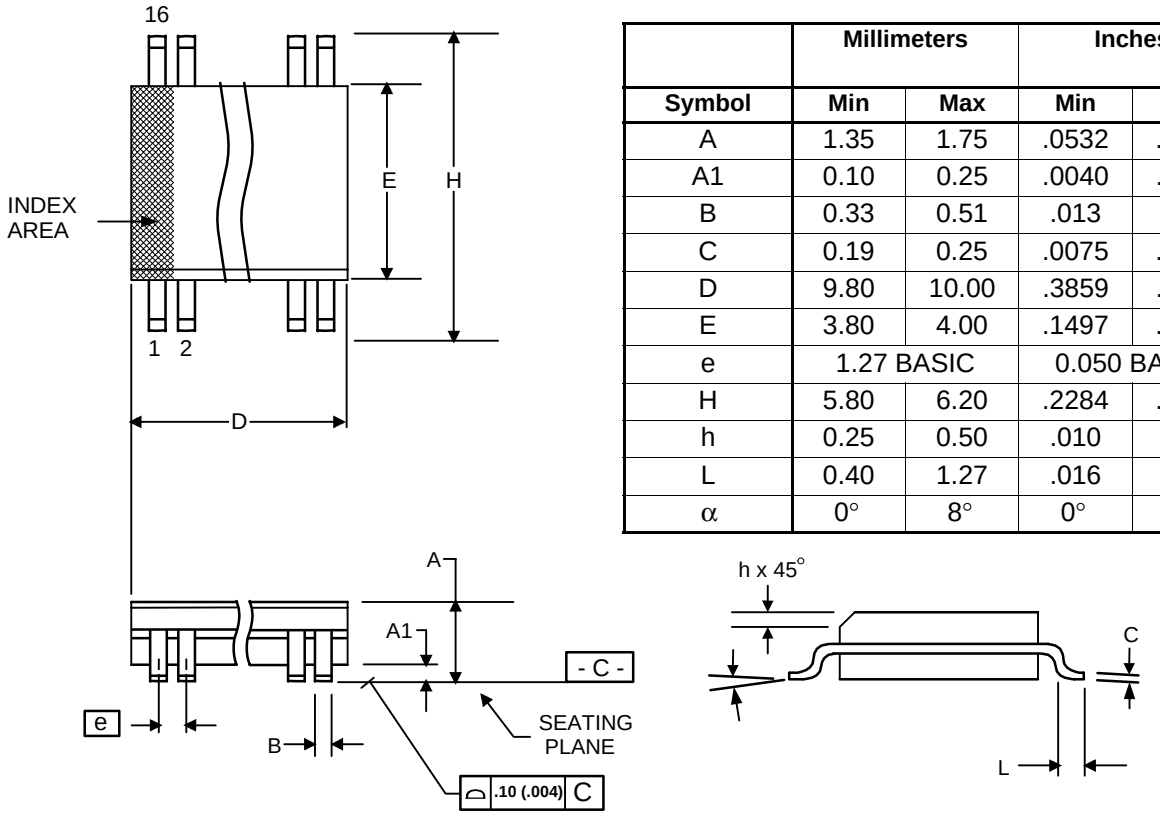
Note 1: The phase relationship between input and output clocks can change at power up. Use the ICS570 or ICS527 Zero Delay Buffers for a guaranteed phase relationship.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		120		°C/W
	θ_{JA}	1 m/s air flow		115		°C/W
	θ_{JA}	3 m/s air flow		105		°C/W
Thermal Resistance Junction to Case	θ_{JC}			58		°C/W

Package Outline and Package Dimensions (16-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	9.80	10.00	.3859	.3937
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
548AM-03LF	548AM-03LF	Tubes	16-pin SOIC	0 to +70° C
548AM-03LFT	548AM-03LF	Tape and Reel	16-pin SOIC	0 to +70° C
548AMI-03LF	548AMI03LF	Tubes	16-pin SOIC	-40 to +85° C
548AMI-03LFT	548AMI03LF	Tape and Reel	16-pin SOIC	-40 to +85° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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