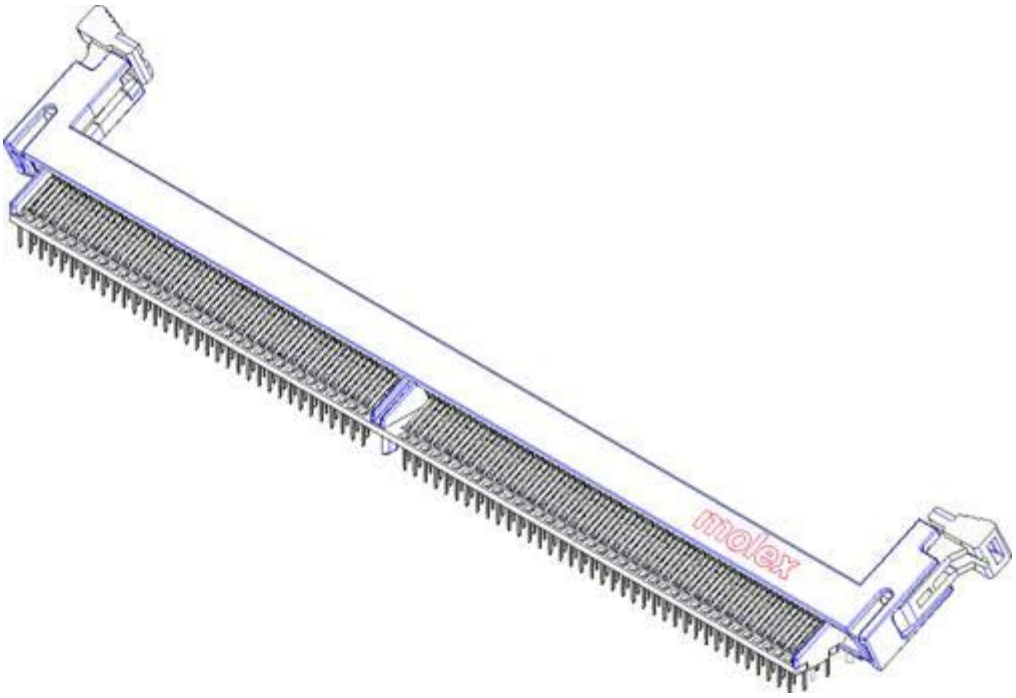
TEST SUMMARY

SIGNAL INTEGRITY TEST SUMMARY

DDR4 DIMM 0.85MM PITCH 25 DEGREES CONNECTOR



1.0 SCOPE

This test summary covers the signal integrity performance of DDR4 DIMM 0.85mm Pitch 25 Degrees through-hole connector. The measurement was conducted using Molex DDR4 Angled 25 Degrees test fixture. Most of the test fixture effect was removed using AFR in PLTS.

2.0 PRODUCT DESCRIPTION

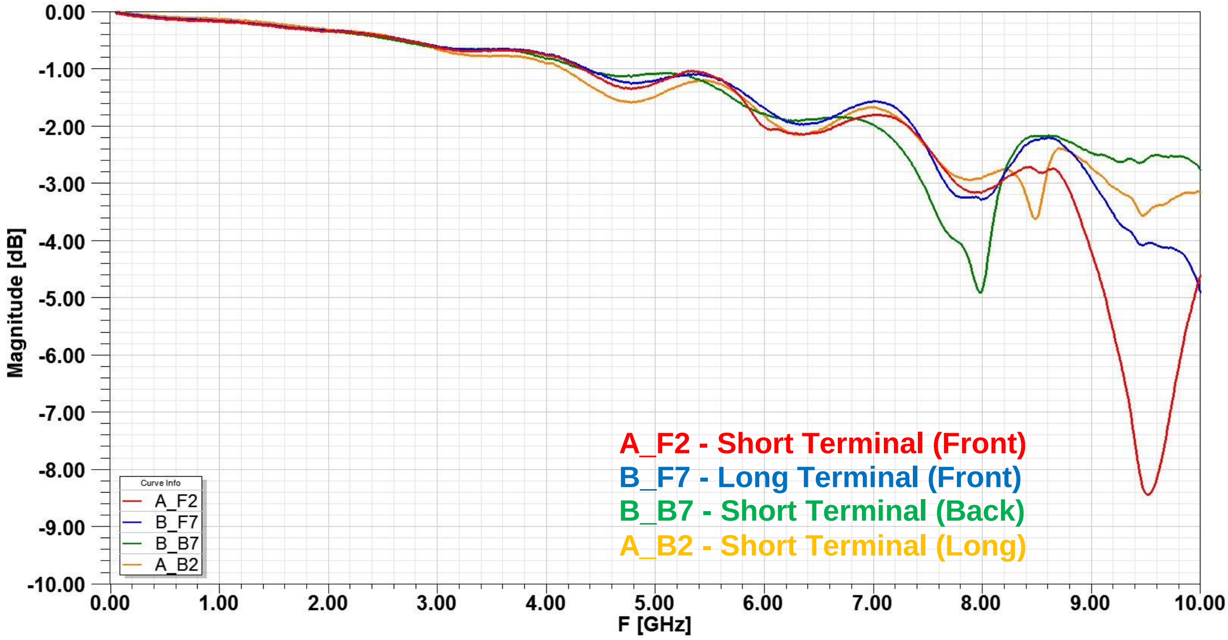
2.1 PRODUCT NAME AND PART NUMBER

DDR4 DIMM 0.85mm Pitch 25 Degrees through-hole connector, Part # 151080-0101.

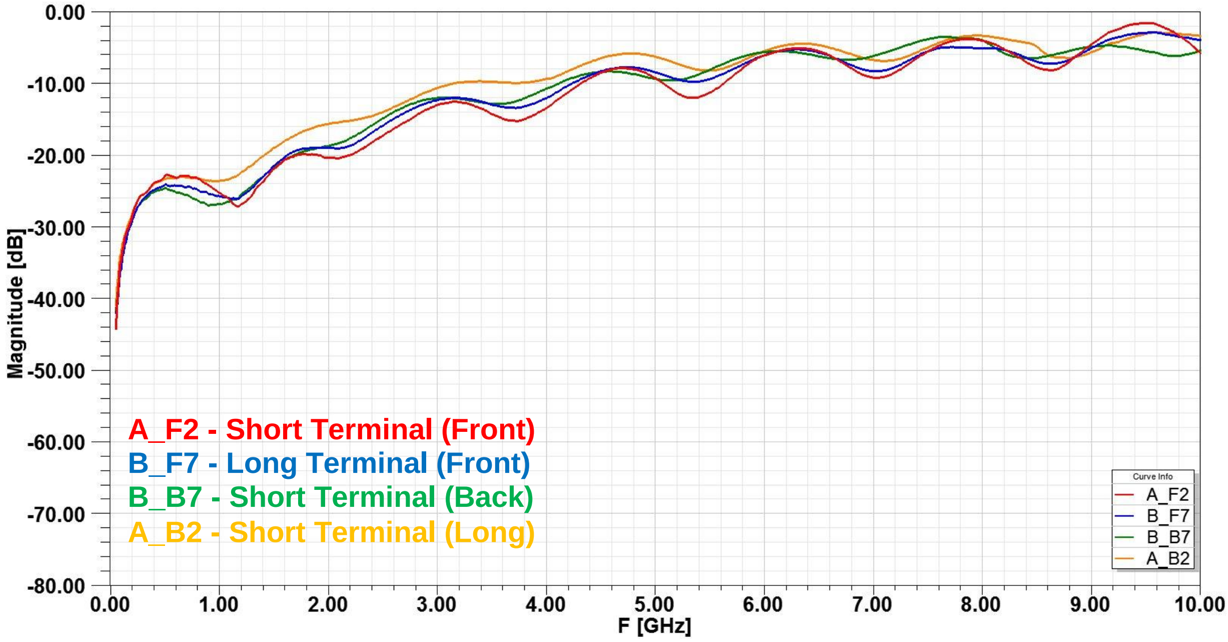
3.0 PERFORMANCE

Frequency Domain

Insertion Loss



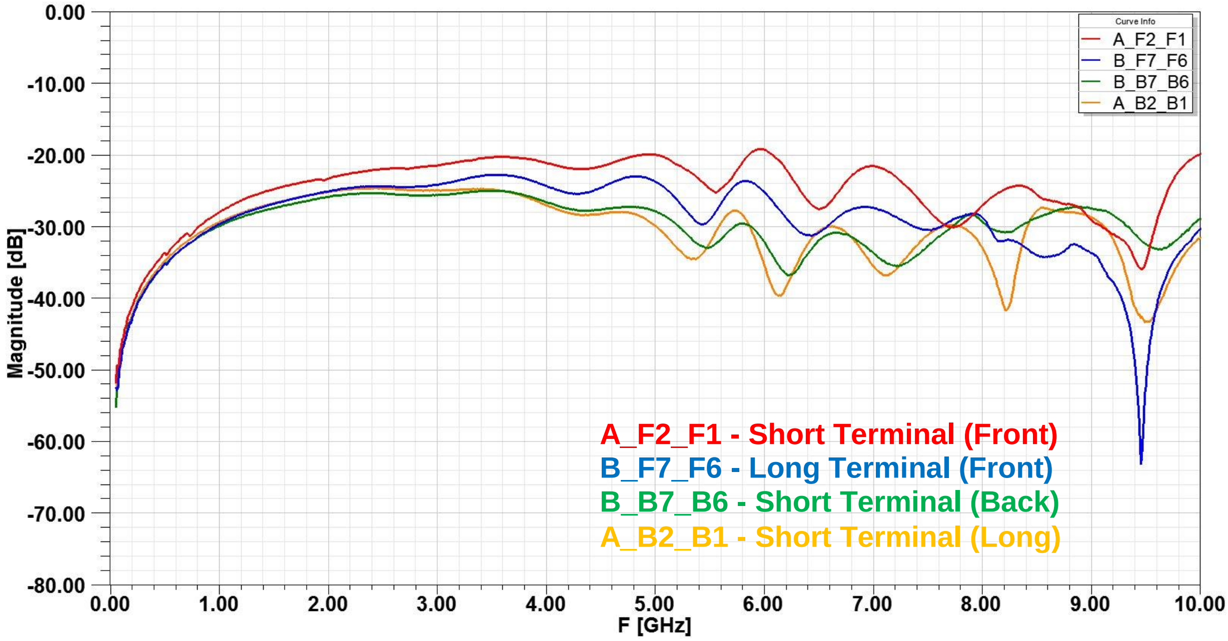
Return Loss



Frequency Domain (continued)

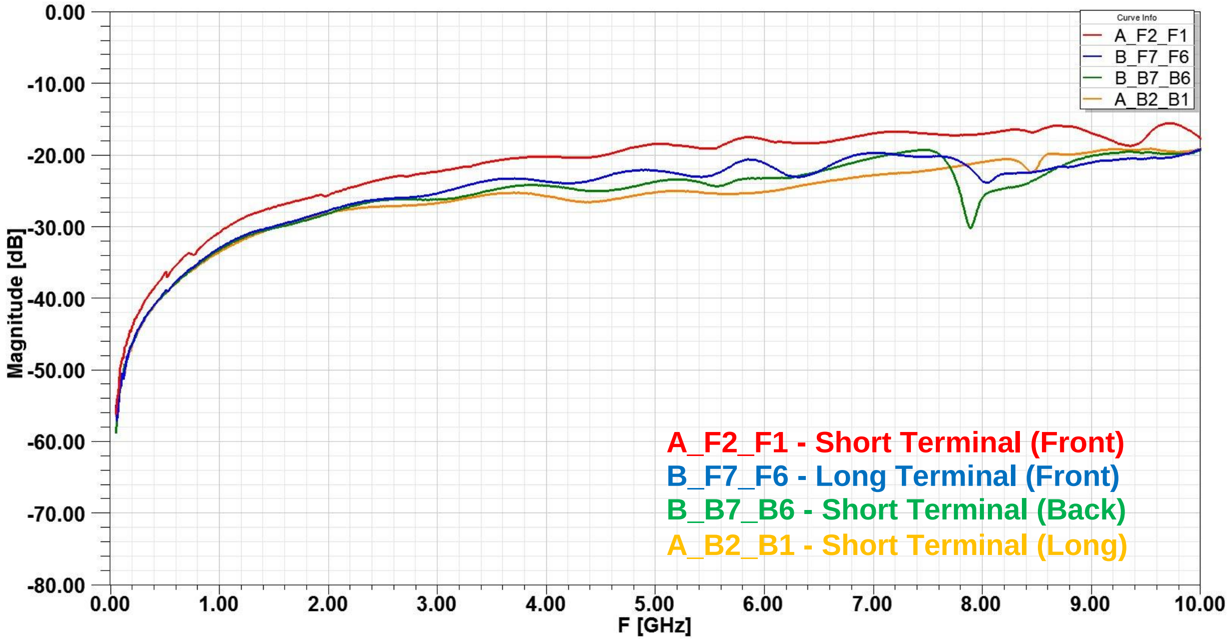
Near End Cross-Talk (Same Side)

- 1:1 S/G ratio
- Both victim and aggressor located at same row



Far End Cross-Talk (Same Side)

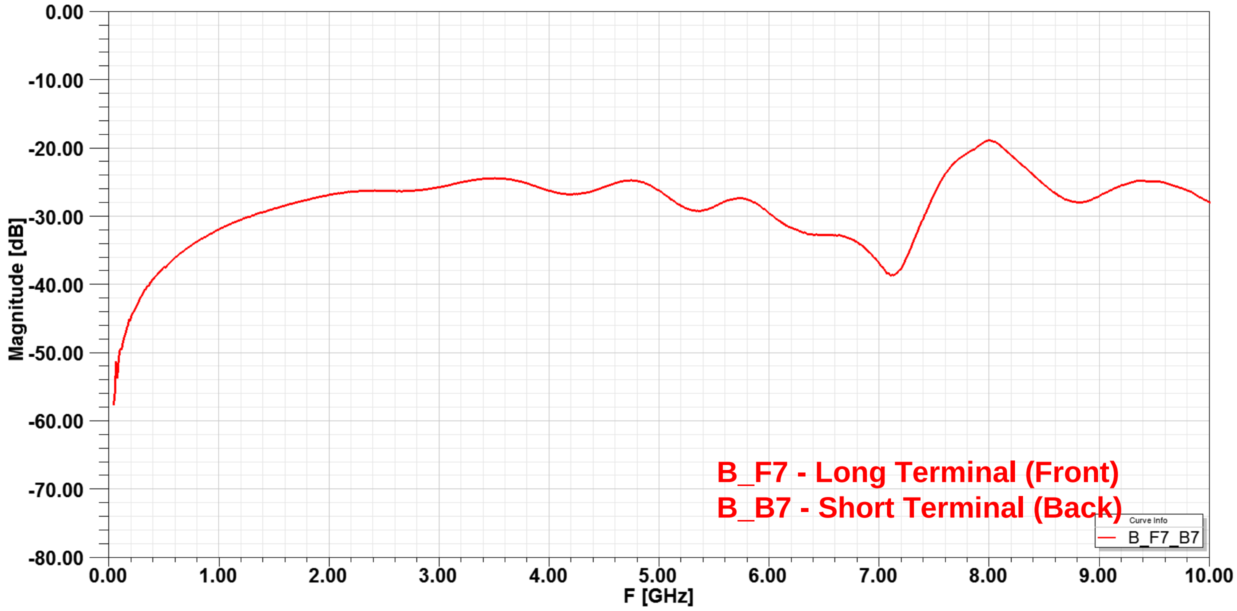
- 1:1 S/G ratio
- Both victim and aggressor located at same row



Frequency Domain (continued)

Near End Cross-Talk (Opposite Side)

- 1:1 S/G ratio
- Victim locates at inner row from front side
- Aggressor locates at inner row from back side



B_F7 - Long Terminal (Front)
B_B7 - Short Terminal (Back)

Far End Cross-Talk (Opposite Side)

- 1:1 S/G ratio
- Victim locates at inner row from front side
- Aggressor locates at inner row from back side.
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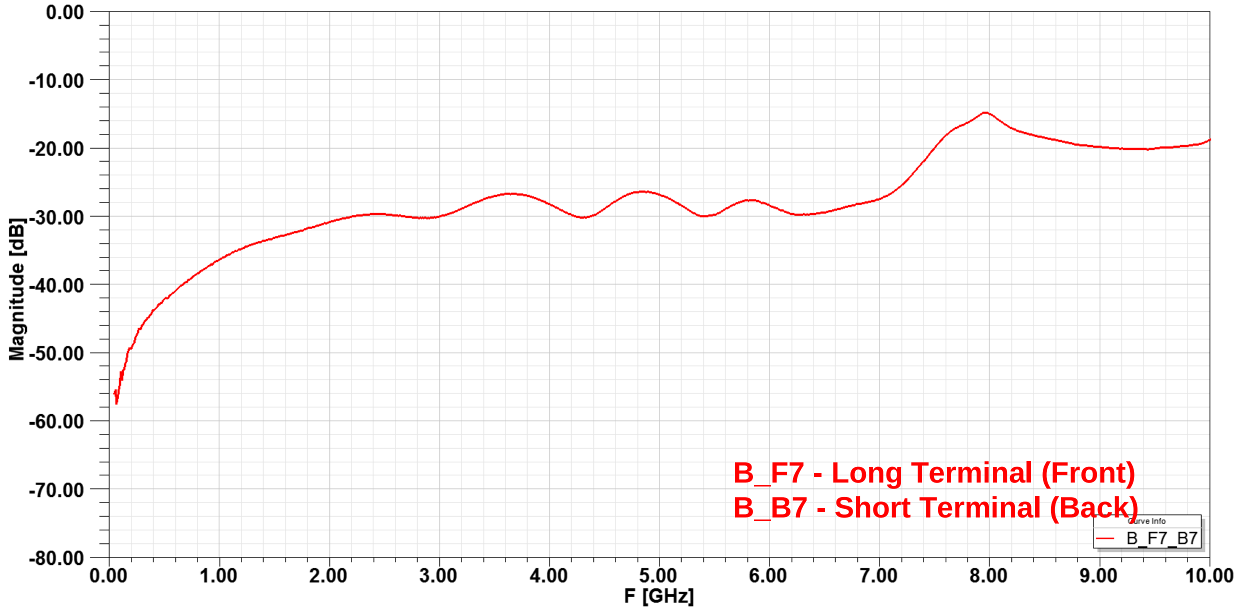
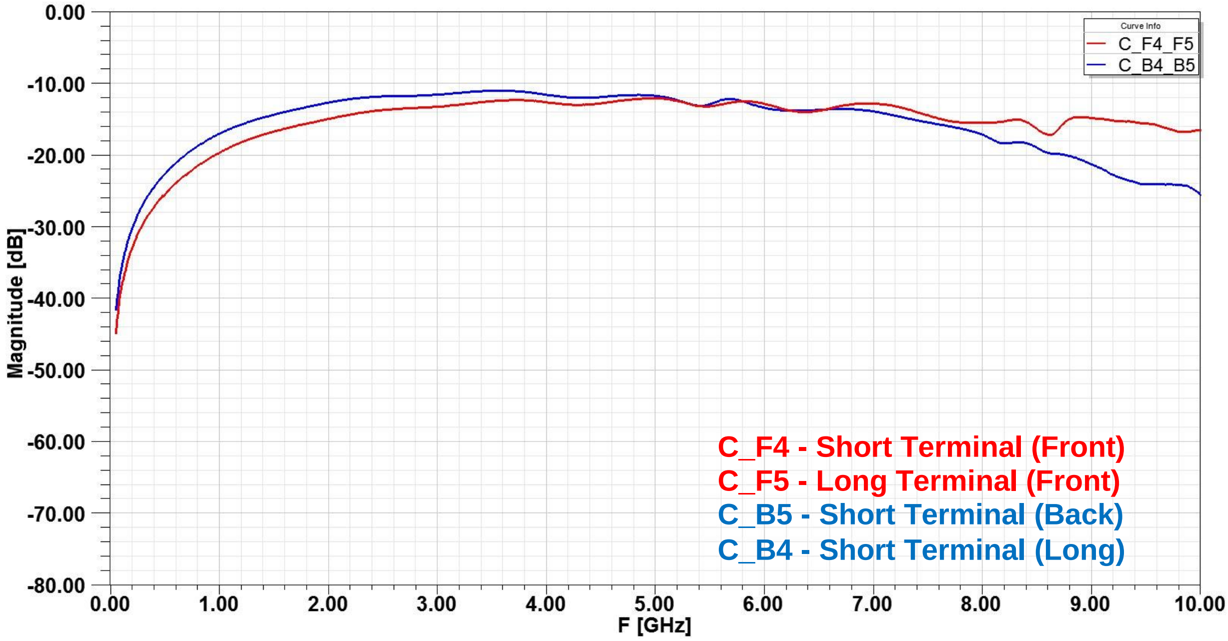


B_F7 - Long Terminal (Front)
B_B7 - Short Terminal (Back)

Frequency Domain (continued)

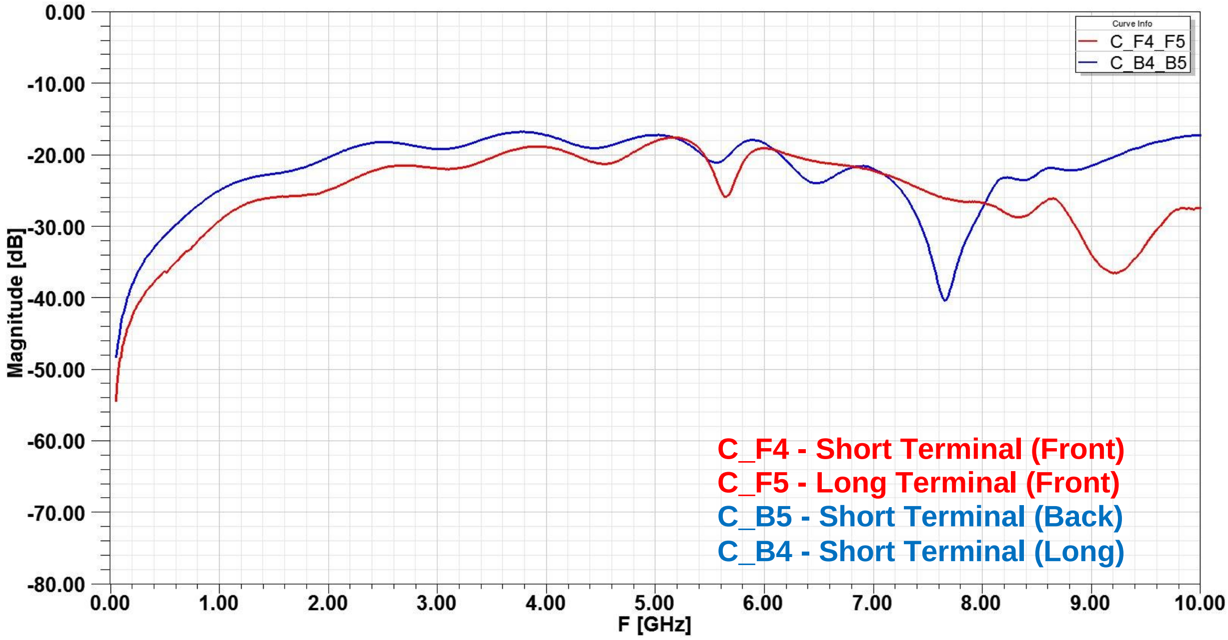
Near End Cross-Talk (Same Side)

- 2:1 S/G ratio



Far End Cross-Talk (Same Side)

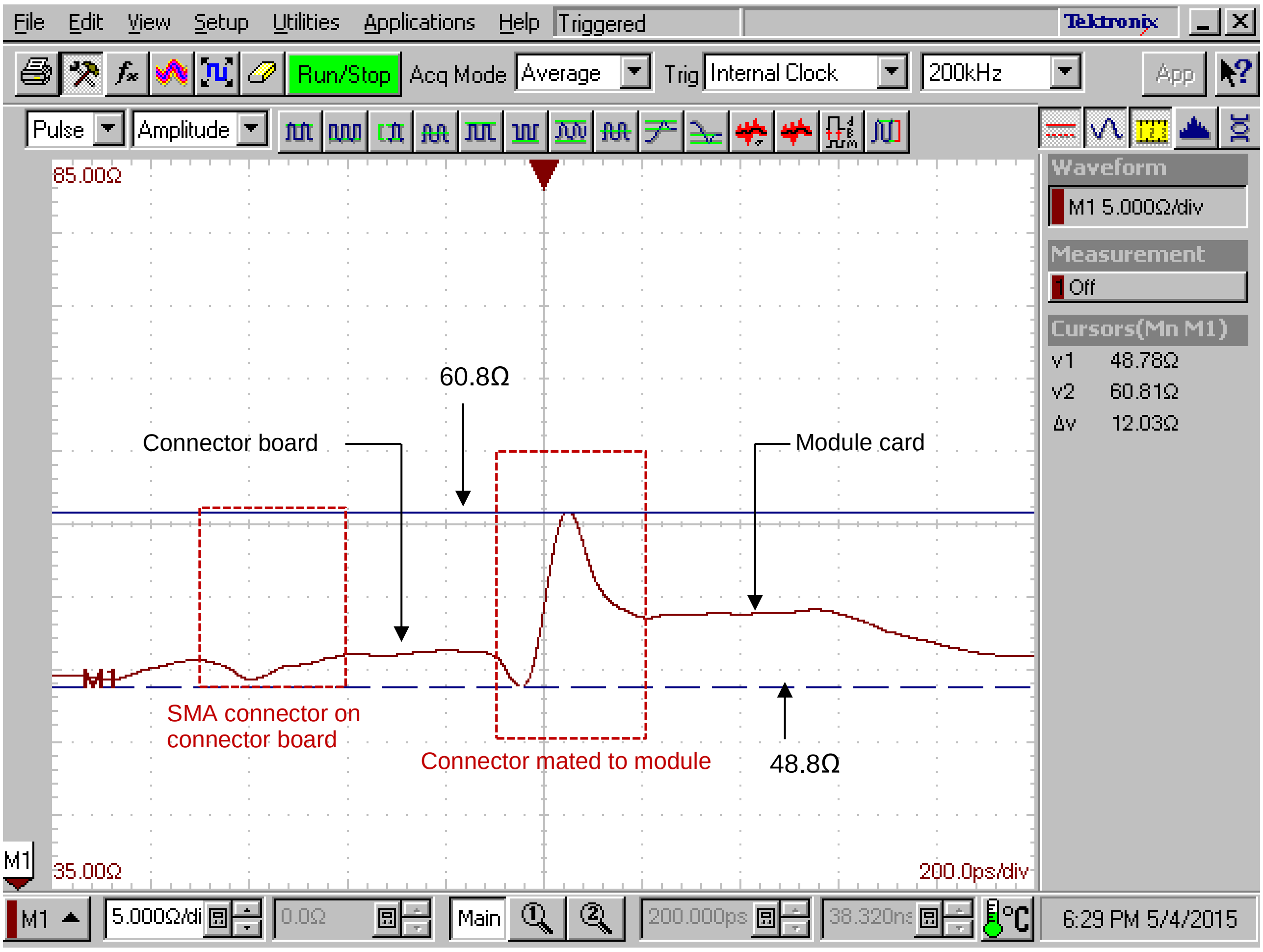
- 2:1 S/G ratio



Time Domain

TDR Impedance

- A_F2 – Short terminal (Front)
- Referenced rise-time of 100ps [10%~90%] launched at connector footprint

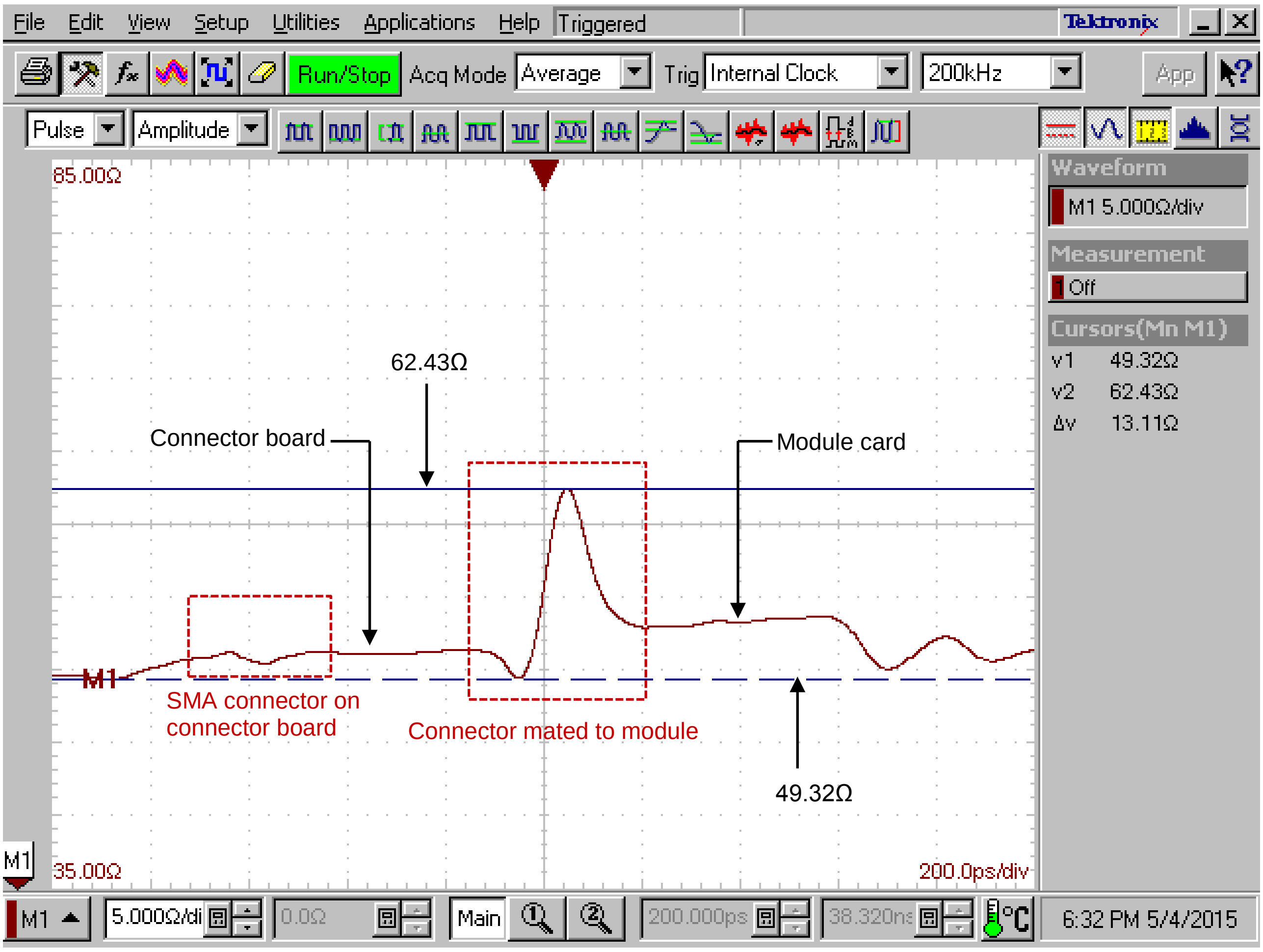


v1 48.78Ω
v2 60.81Ω
Δv 12.03Ω

Time Domain (continued)

TDR Impedance

- B_F7 – Long terminal (Front)
- Referenced rise-time of 100ps [10%~90%] launched at connector footprint



Triggered

Acq Mode Average

Trig Internal Clock

200kHz

Pulse

Amplitude

Waveform

M1 5.000Ω/div

Measurement

Off

Cursors(Mn M1)

v1 49.32Ω

v2 62.43Ω

Δv 13.11Ω

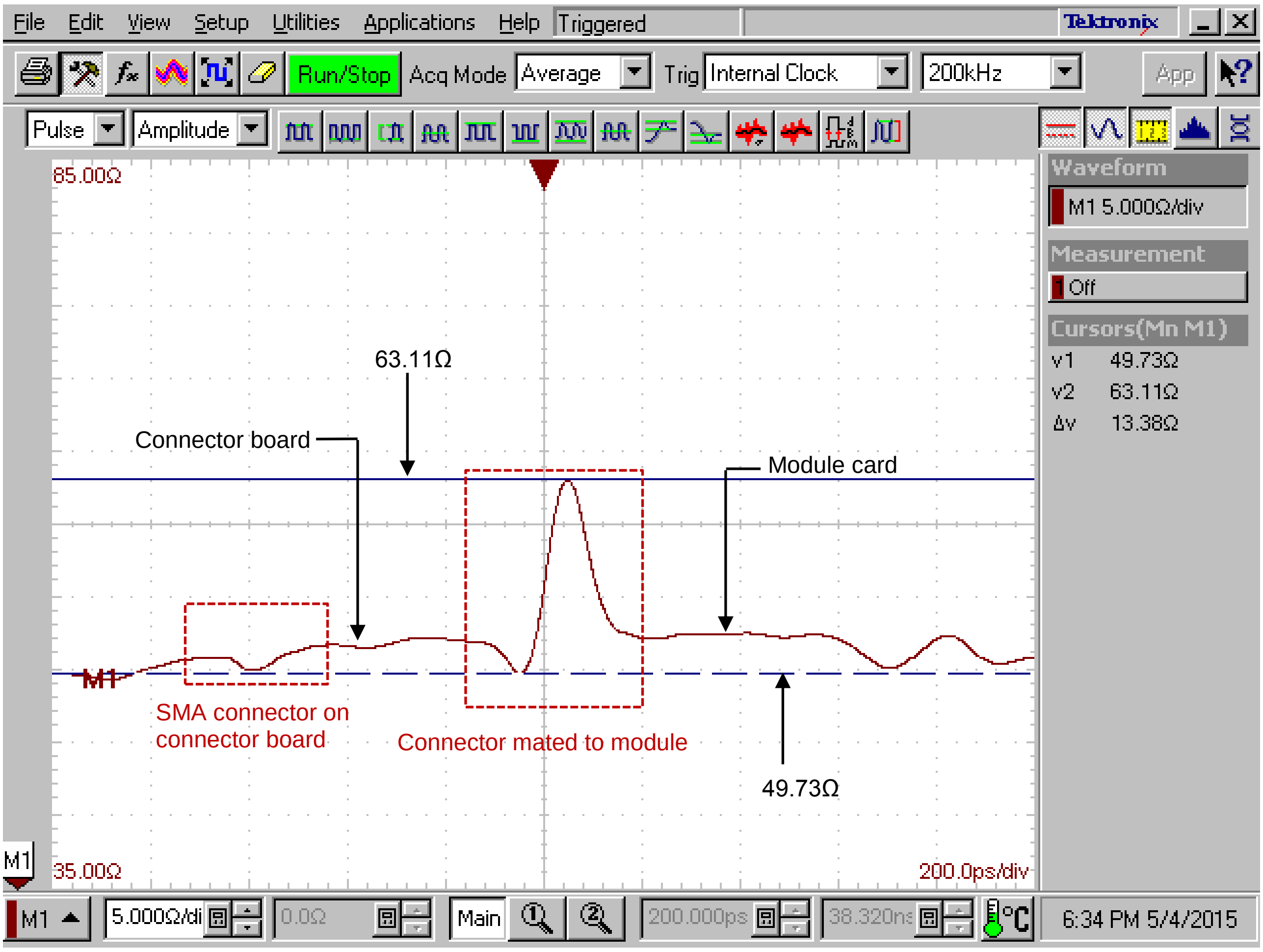
M1 5.000Ω/di 0.0Ω 200.000ps 38.320ns

6:32 PM 5/4/2015

Time Domain (continued)

TDR Impedance

- B_B7 – Short terminal (Back)
- Referenced rise-time of 100ps [10%~90%] launched at connector footprint



Acq Mode Average
Trig Internal Clock
200kHz
Pulse
Amplitude

M1 5.000Ω/div
Measurement Off

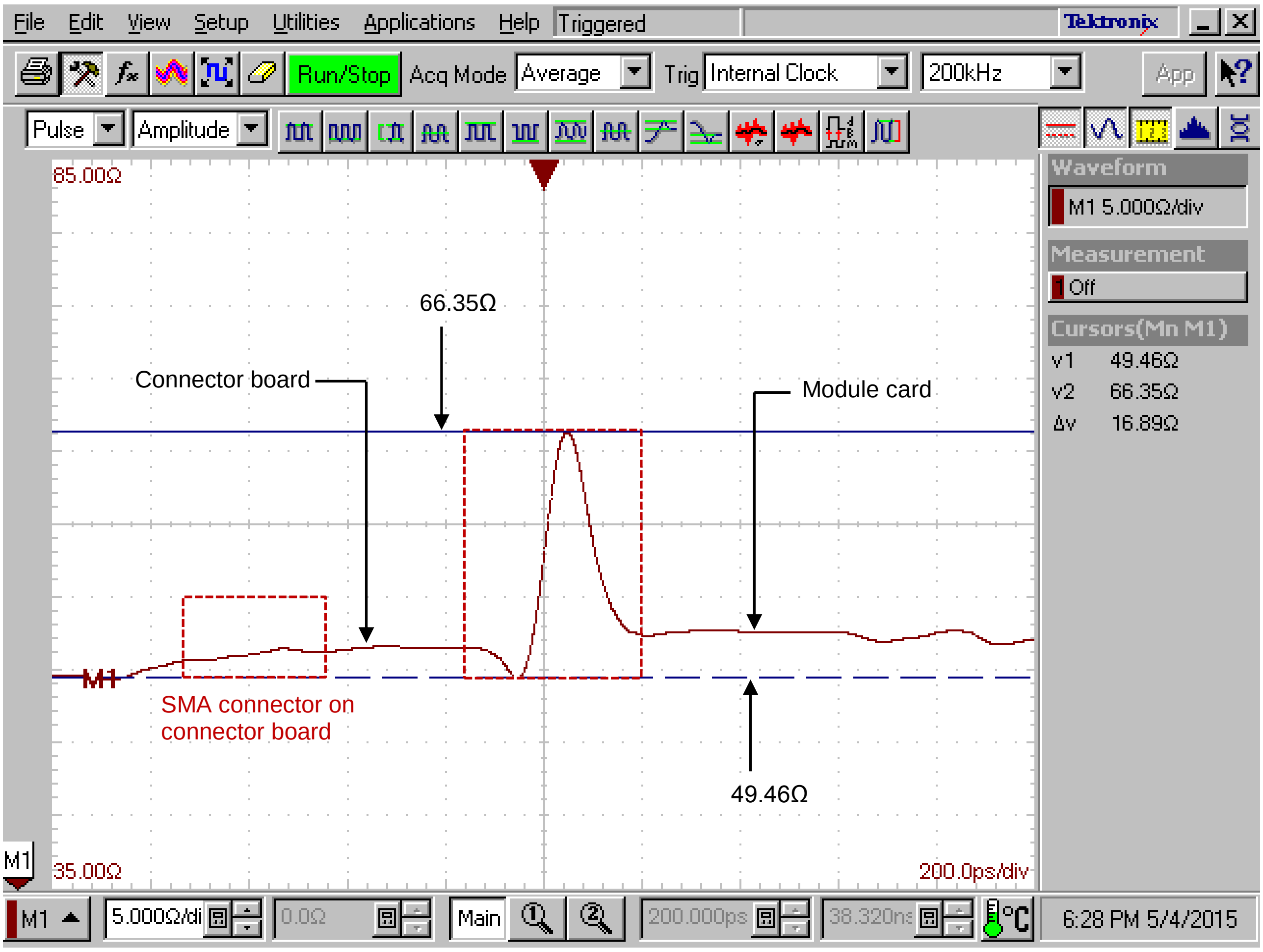
Cursors(Mn M1)
v1 49.73Ω
v2 63.11Ω
Δv 13.38Ω

M1 5.000Ω/di 0.0Ω Main 200.000ps 38.320ns °C 6:34 PM 5/4/2015

Time Domain (continued)

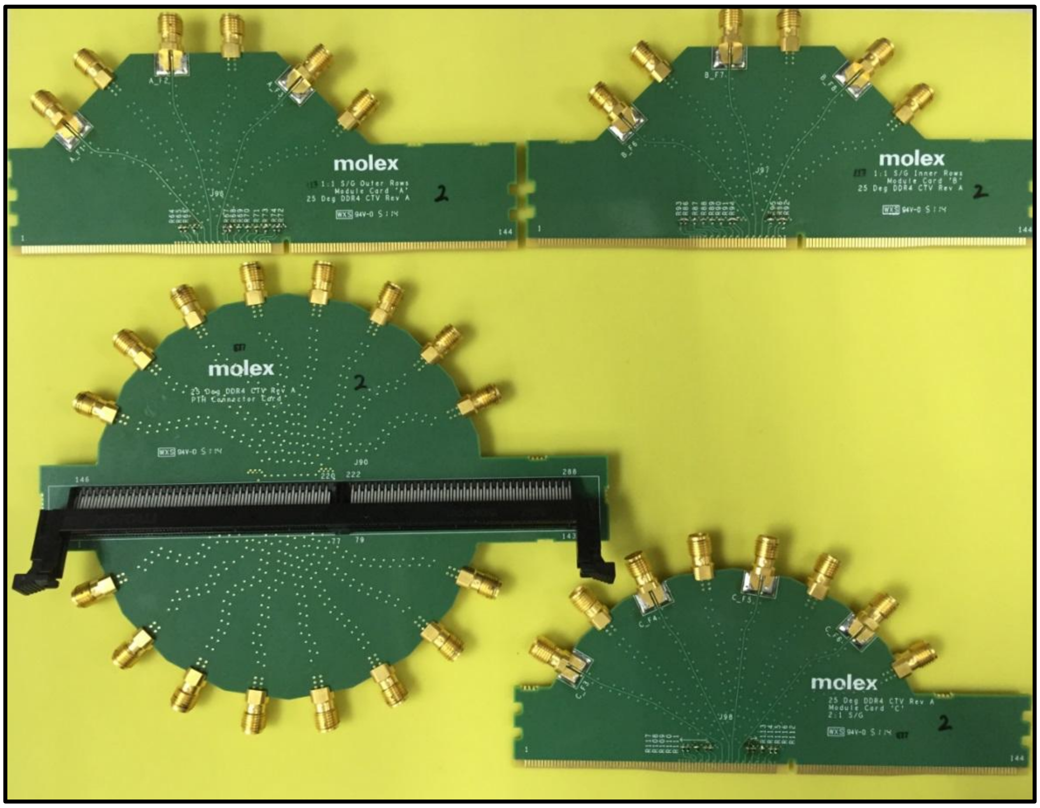
TDR Impedance (A_B2)

- A_B2 – Long terminal (Back)
- Referenced rise-time of 100ps [10%~90%] launched at connector footprint



Acq Mode: Average
Trig: Internal Clock
200kHz
Pulse
Amplitude
M1 5.000Ω/div
Measurement: Off
v1 49.46Ω
v2 66.35Ω
Δv 16.89Ω
M1 5.000Ω/di
0.0Ω
200.000ps
38.320ns
6:28 PM 5/4/2015

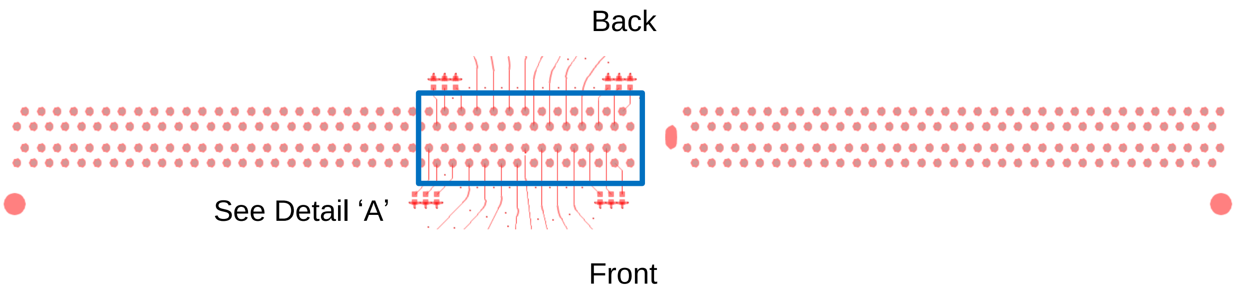
4.0TEST FIXTURES



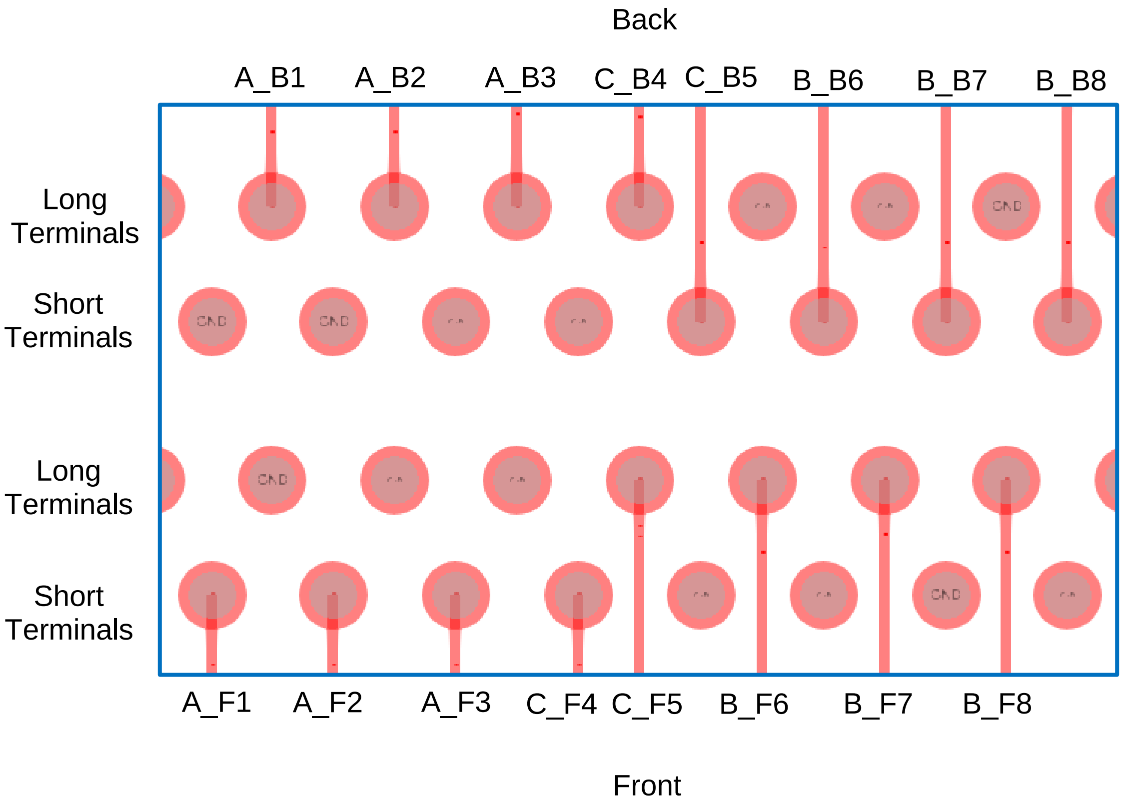
<u>Molex DDR4 Test Fixture Board Information</u>

Material :	TU-872-SLK
Thickness :	1.4mm
High Speed Traces :	High-Speed Signals on Top Layer (referenced to Layer 2) and Bottom Layer (referenced to Layer 3) 0.09398mm dielectric thickness between Top Layer & Layer 2 ; Layer 3 & Bottom Layer 50.8mm single-ended length (both main and module board)

Mainboard Footprint Detail



Detail ‘A’



REVISION: **B**	ECN INFORMATION: EC No: **S2015-1365** DATE: **2015/05/22**	TITLE: **Signal Integrity Test Summary** **DDR4 DIMM 0.85MM PITCH** **25 Deg T/H CONNECTOR** **MOLEX CONFIDENTIAL**	SHEET No. **11** of **11**
DOCUMENT NUMBER: **TS-151080-0001**	CREATED / REVISED BY: **WHFOO 2015/05/22**	CHECKED BY: **CMWONG 2015/05/22**	APPROVED BY: **WTCHUA 2015/05/22**