PIC16C433

PIC16C433 Data Sheet Errata

The PIC16C433 parts you have received conform functionally to the Device Data Sheet (DS41139**A**), except for the anomalies described below.

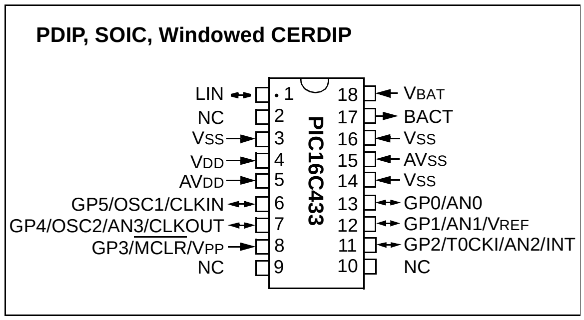
None.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS41139**A**), the following clarifications and corrections should be noted.

The Pin Diagram shown on page 1 of the Data Sheet has been changed with pin 2 renamed, as shown in the following figure:

PIN DIAGRAM



Note:	Pins designated ‘NC’ have no internal connection to the device.

The description of the BACT (Bus activity output) function in Table 3-1 has changed. Refer to updated Table 3-1:

TABLE 3-1: PIC16C433 PINOUT DESCRIPTION

Name	DIP Pin #	I/O/P Type	Buffer Type	Description
GP0/AN0	13	I/O	TTL/ST	Bi-directional I/O port/serial programming data/analog input 0. Can be software programmed for internal weak pull-up and interrupt-on-pin change. This buffer is a Schmitt Trigger input when used in Serial Programming mode.
GP1/AN1/VREF	12	I/O	TTL/ST	Bi-directional I/O port/serial programming clock/analog input 1/voltage reference. Can be software programmed for internal weak pull-up and interrupt-on-pin change. This buffer is a Schmitt Trigger input when used in Serial Programming mode.
GP2/T0CKI/AN2/INT	11	I/O	ST	Bi-directional I/O port/analog input 2. Can be configured as T0CKI or external interrupt.
GP3/$\overline{MCLR}$/VPP	8	I	TTL/ST	Input port/Master Clear (Reset) input/programming voltage input. When configured as $\overline{MCLR}$, this pin is an active low RESET to the device. Voltage on $\overline{MCLR}$/VPP must not exceed VDD during normal device operation. Can be software programmed for internal weak pull-up and interrupt-on-pin change. Weak pull-up always on if configured as $\overline{MCLR}$. This buffer is Schmitt Trigger when in $\overline{MCLR}$ mode.
GP4/OSC2/AN3/CLKOUT	7	I/O	TTL	Bi-directional I/O port/oscillator crystal output/analog input 3. Connections to crystal or resonator in Crystal Oscillator mode (HS, XT and LP modes only, GPIO in other modes). In EXTRC and INTRC modes, the pin output can be configured to CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
GP5/OSC1/CLKIN	6	I/O	TTL/ST	Bi-directional IO port/oscillator crystal input/external clock source input (GPIO in INTRC mode only, OSC1 in all other oscillator modes). Schmitt Trigger input for EXTRC Oscillator mode.
LIN	1	I/O	HV/OD	High voltage bi-directional bus interface.
VBAT	18	P	—	Battery input voltage.
BACT	17	O	—	Bus activity output pin. No connection if not used. It is a CMOS-levels representation of the LIN pin.
VDD	4	P	—	Positive supply for logic and I/O pins.
VSS	3,14,16	P	—	Ground reference for logic and I/O pins.
AVDD	5	P	—	Analog positive supply.
AVSS	15	P	—	Analog ground.

Legend: I = Input, O = Output, I/O = Input/Output, P = Power, — = not used, TTL = TTL input,
ST = Schmitt Trigger input, OD = Open Drain

Page 25 of the Data Sheet, Section 5.4 The BACT Pin, has been changed to the following:

5.4 The BACT Pin

The BACT pin can be used to wake-up the device from SLEEP upon bus activity. In order to wake the bus up, the BACT pin has to be tied to one of the GPIO<0:3> pins. Any one of the four GPIO pins can be used for wake-up where GPIO<2> is an external interrupt which offers multiple configuration options (Section 9.5.2 of Data Sheet) and GPIO<0:1,3> are interrupt-on-change (Section 9.5.3 of Data Sheet). The BACT output is a CMOS- levels representation of the LIN pin. This pin is not latched.

Page 33 of the Data Sheet, Section 6.2 LIN Bus Interfacing, Section 6.3 LIN Bus Hardware Interface, and Section 6.5 Wake-up from SLEEP upon Bus Activity, have been changed to the following:

6.2 LIN Bus Interfacing

The LIN protocol is implemented and programmed by the user, using the LINTX and LINRX bits, which are used to interface to the transceiver. The LIN Bus firmware transmits by toggling the LINTX bit in the GPIO register and is read by reading the LINRX bit in the GPIO register. All aspects of the protocol are handled by software (i.e. bit-banged), where the transceiver is used as the physical interface to the LIN Bus network.

For an interrupt based LIN Bus slave implementation, please refer to AN729, available on Microchip's website (www.microchip.com). This application note is based on PIC16C622, but can be converted for either PIC16C432 or PIC16C433.

For the PIC16C433, the changes required include but are not limited to:

1. Change the include file to "`p16C433.inc`".
2. Use LINTX bit in GPIO register instead of TXLINEPIN in PORTB to transmit.
3. Use LINRX bit in GPIO register instead of TXLINEPIN in PORTB to receive.
4. Connect the bus to LIN pin to receive and transmit instead of PORTB<0> and PORTB<4>.

The transceiver in the PIC16C433 uses the microcontroller's dual-die interface; therefore, the software must initialize the LINTX and LINRX bits to a '1' before each LIN communication. If the LINTX bit is left cleared (e.g. CLRF GPIO), no other nodes on the network will be able to communicate on the LIN Bus until LINTX is set to '1' for '0' is the dominate state for the protocol.

EXAMPLE 6-1: INITIALIZING LINTX AND LINRX BITS

```
MOVLW    H'C0'
MOVWF    GPIO
```

It is recommended that the firmware verify each bit transmitted, by comparing the LINTX and LINRX bits, to ensure no bus contention or hardware failure has occurred. The LINTX and LINRX bits have no associated TRIS bits. Therefore, LINTX is always an output and LINRX is always an input.

6.3 LIN Bus Hardware Interface

Figure 6-1 shows how to implement the hardware LIN Bus interface in a master configuration and Figure 6-2 in a slave configuration using the PIC16C433. Figure 6-3 shows how to implement the hardware for a master configuration using BACT pin to generate a wake-up interrupt using GP2. The transceiver has an internal series resistor and diode, as defined in the LIN 1.2 specification, connecting V_{BAT} and LIN pin.

Note:	No resistor is required between V_{BAT} pin and 12V supply and for slave configuration, no resistor is required between V_{BAT} and LIN.

6.5 Wake-up from SLEEP upon Bus Activity

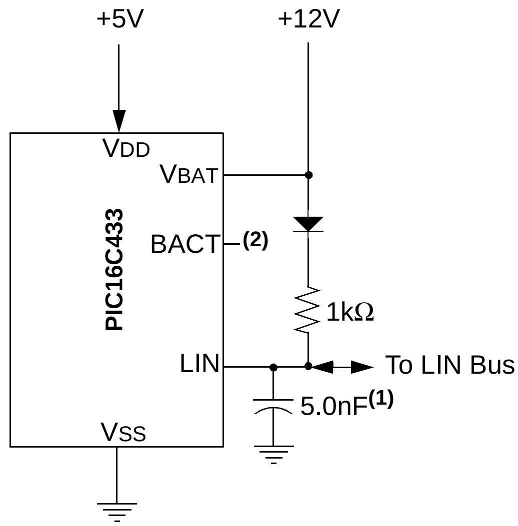
The PIC16C433 can wake-up from SLEEP upon bus activity in the following way:

1. Connect BACT to one of GPIO<0:3> pins.

The BACT output is a CMOS-levels representation of the LIN pin. This signal can be routed to one of the GPIO<0:3> pins. The GPIO<2> external interrupt or GPIO<0:1,3> interrupt-on-change wakes up the device from SLEEP. Any one of the four GPIO pins can be used for wake-up where GPIO<2> offers multiple configuration options (Section 9.5.2 of Data Sheet) and GPIO<0:1,3> are interrupt-on-change (Section 9.5.3 of Data Sheet).

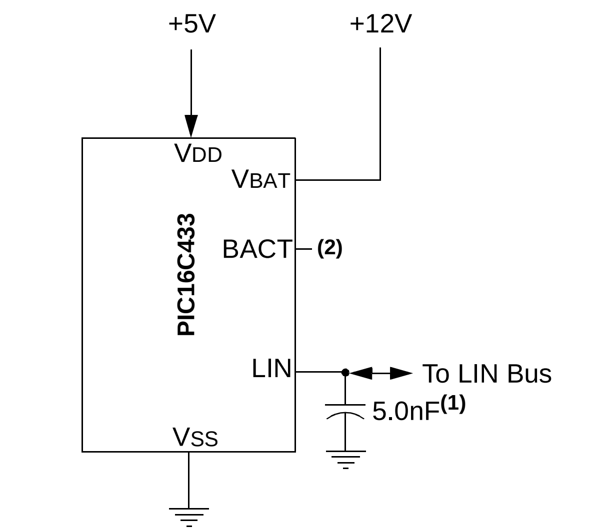
Note:	BACT pin is an output and must be left open if unused.

FIGURE 6-1: TYPICAL LIN BUS MASTER APPLICATION



Note 1: May not be required.
2: BACT pin should be left open if not used.

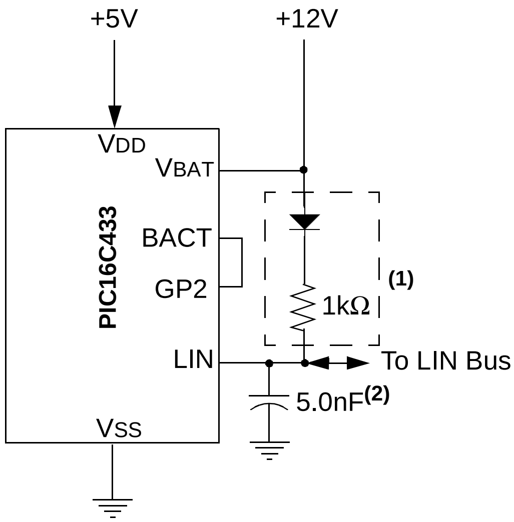
FIGURE 6-2: TYPICAL LIN BUS SLAVE APPLICATION



Note 1: May not be required.
2: BACT pin should be left open if not used.

A new figure has been added to show connections using Wake-up interrupt, Figure 6-3:

FIGURE 6-3: LIN BUS APPLICATION USING WAKE-UP INTERRUPT



Note 1: For master configuration only.
2: May not be required.

TABLE 6-1: SUMMARY OF LIN BUS TRANSCEIVER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR	Value on All Other RESETS
05h	GPIO	LINTX	LINRX	GP5	GP4	GP3	GP2	GP1	GP0	11xx xxxx	11uu uuuu

Legend: x = unknown, u = unchanged. Shaded cells not used by LIN Transceiver.

The Electrical Specifications have been changed to include the maximum current sunk by LIN and BACT pins, as shown in the following table in Section 12.0 of the PIC16C433 Data Sheet.

12.0 Electrical Specifications for PIC16C433

Absolute Maximum Ratings (†)

Ambient Temperature under bias	-40° to +125°C
Storage Temperature	-65° to +150°C
Voltage on any pin with respect to V_{SS} (except V_{DD} and $\overline{MCLR}$)	-0.6V to V_{DD} +0.6V
Voltage on V_{DD} with respect to V_{SS}	0 to +7.0V
Voltage on RA4 with respect to V_{SS}	8.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} **(Note 2)**	0 to +14V
Voltage on RA4 with respect to V_{SS}	8.5V
Total power Dissipation **(Note 1)**	1.0W
Maximum Current out of V_{SS} pin	300 mA
Maximum Current into V_{DD} pin	250 mA
Input Clamp Current, I_{IK} (V_I <0 or V_I> V_{DD})	±20 mA
Output Clamp Current, I_{OK} (V_O <0 or V_O>V_{DD})	±20 mA
Maximum Output Current sunk by any I/O pin	25 mA
Maximum Output Current sourced by any I/O pin	25 mA
Maximum Current sunk by GPIO	200 mA
Maximum Current sourced by GPIO	200 mA
Maximum Current sunk by LIN	200 mA
Maximum Current sunk by BACT	1.8 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{Ol} \times I_{OL})$

2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin, rather than pulling this pin directly to V_{SS}.

† **NOTICE**: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

APPENDIX A: REVISION HISTORY

Rev. A Document (9/2001)

First revision of this document.

Under Clarifications/Corrections to the Data Sheet, corrections have been made to the following:

PIN DIAGRAM - renamed Pin 2.

TABLE 3-1 - description of the BACT function.

Section 5.4 - change to BACT Pin.

Section 6.2 - LIN Bus Interfacing.

Section 6.3 - LIN Bus Hardware Interface.

Section 6.5 - Wake-up from SLEEP upon Bus Activity.

FIGURE 6.3 - added to show connections using Wake-up interrupt.

12.0 Electrical Specifications for PIC16C433 - changed to include the maximum current sunk by LIN and BACT pins.

Rev. B Document (10/2001)

Change title of document from Rev. B Silicon Errata to Data Sheet Errata. Deleted ‘Rev. C’ from first paragraph, page 1.

Note the following details of the code protection feature on PICmicro® MCUs.

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