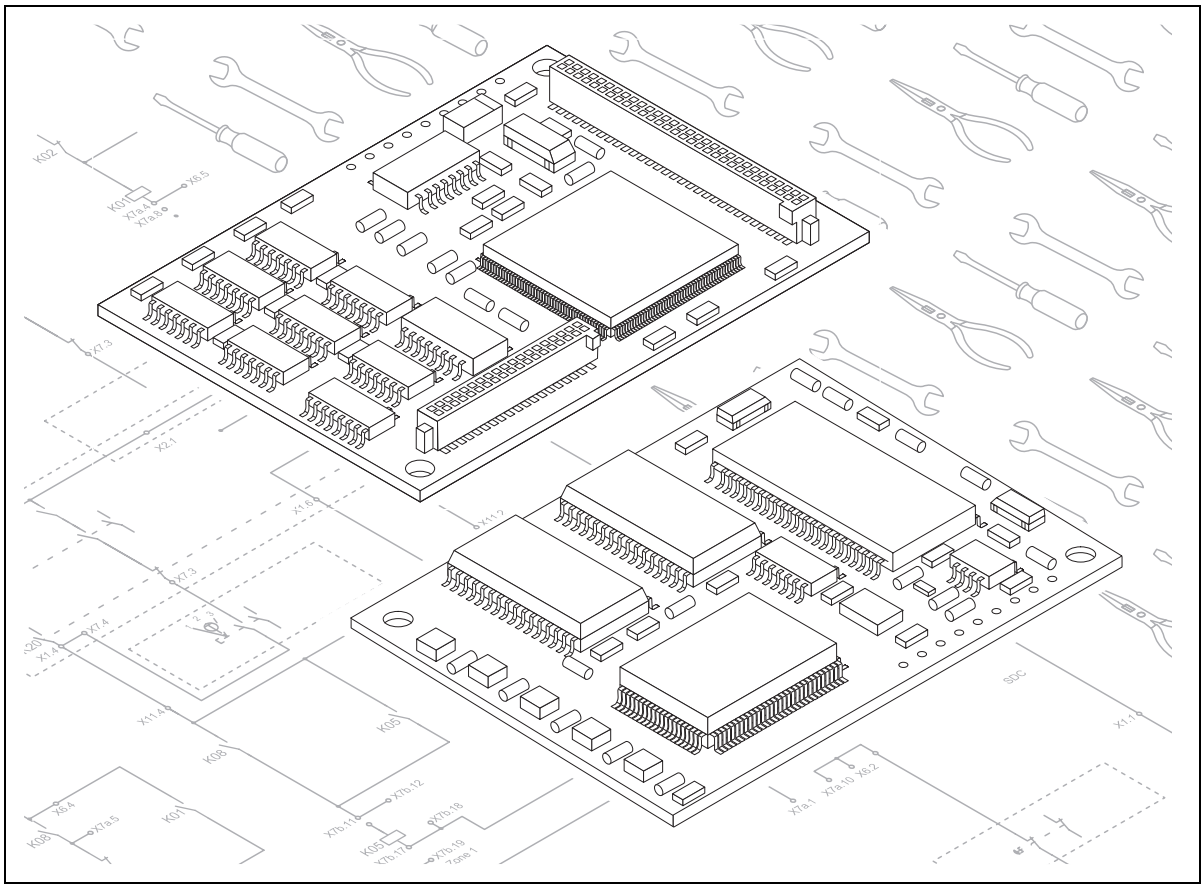
PHOENIX CONTACT

INNOVATION IN INTERFACE

User Manual

INTERBUS Generation 4 Master Board

Designation: IBS USC4-2 UM E



User Manual

INTERBUS Generation 4 Master Board

Designation: IBS USC4-2 UM E

Revision: 01

This manual is valid for:

IBS USC4-2 Order No. 28 12 20 9

© Phoenix Contact 04/2005

653801

Please Observe the Following Notes

In order to guarantee the safe use of your device, we recommend that you read this manual carefully. The following notes give you information on how to use this manual.

Qualifications of the User Group

The products described in this manual should be installed/operated/maintained only by electricians or persons instructed by them, who are familiar with applicable national standards. Phoenix Contact assumes no liability for damage to any products resulting from disregard of information contained in this manual.

Explanation of Symbols Used

The *attention* symbol refers to an operating procedure which, if not carefully followed, could result in damage to equipment or personal injury.

The *note* symbol informs you of conditions that must strictly be observed to achieve error-free operation. It also gives you tips and advice on hardware and software optimization to save you extra work.

The *text* symbol refers you to detailed sources of information (manuals, data sheets, literature, etc.) on the subject matter, product, etc. This text also provides helpful information for the orientation in the manual.

We Are Interested in Your Opinion

We are constantly striving to improve the quality of our documents.

Should you have any suggestions or recommendations for improving the contents and layout of our documents, please send us your comments. Please use the fax form at the end of the manual for this purpose.

General Terms and Conditions of Use for Technical Documentation

Phoenix Contact GmbH & Co. KG reserves the right to alter, correct, and/or improve the technical documentation and the products described in the technical documentation at its own discretion and without giving any notice.

The receipt of technical documentation (in particular data sheets, installation instructions, manuals, etc.) does not constitute any further duty on the part of Phoenix Contact GmbH & Co. KG to furnish information on alterations to products and/or technical documentation. Any other agreement shall only apply if expressly confirmed in writing by Phoenix Contact GmbH & Co. KG.

Although Phoenix Contact GmbH & Co. KG makes every effort to ensure that the information content is accurate, up-to-date and state-of-the-art, technical inaccuracies and/or printing errors in the information cannot be ruled out.
Phoenix Contact GmbH & Co. KG does not offer any guarantees as to the reliability, accuracy or completeness of the information appearing on the Website.
Phoenix Contact GmbH & Co. KG accepts no liability or responsibility for errors or omissions in the content of the technical documentation (in particular data sheets, installation instructions, manuals, etc.).

As far as is permissible by applicable jurisdiction, no guarantee or claim for liability for defects whatsoever shall be granted in conjunction with the information available in the technical documentation, whether expressly mentioned or implied. This information does not include any guarantees on quality, does not describe any fair marketable quality and does not make any claims as to quality guarantees or guarantees on the suitability for a special purpose. Phoenix Contact GmbH & Co. KG reserves the right to alter, correct, and/or improve the information and the products described in the information at its own discretion and without giving any notice.

Statement of Legal Authority

This manual, including all illustrations contained herein, is copyright protected. Use of this manual by any third party in departure from the copyright provision is forbidden. Reproduction, translation and electronic or photographic archiving or alteration requires the express written consent of Phoenix Contact. Violators are liable for damages.

Phoenix Contact reserves the right to make any technical changes that serve the purpose of technical progress.

Phoenix Contact reserves all rights in the case of patent award or listing of a registered design. External products are always named without reference to patent rights. The existence of such rights shall not be excluded.

Internet

You will find current information on products from Phoenix Contact on the Internet at **www.phoenixcontact.com**.

Table of Contents

1 Contents of This Document

This user manual provides a detailed description of the INTERBUS master board IBS USC4-2. Using the IBS USC4-2 allows for the implementation of INTERBUS masters and INTERBUS master/slave combinations (system couplers).

Section 2 describes the IBS USC4-2 hardware. Wiring of the interfaces is illustrated by means of block diagrams.

Section 3 and Section 4 provide information on how to implement and use a dual-port memory (DPM) as the interface between the IBS USC4-2 and a host system.

The IBS USC/4-DIAG-L diagnostic display and the IBS BD32-ADAPTER programming adapter can be used as useful tools. A master board based on the IBS USC4-2 can be started up immediately using the IBS SWT CMD G4 E software.

The firmware reference manual IBS SYS FW G4 UM E (Order No. 27 45 18 5) describes the firmware of the IBS USC4-2.

2 IBS USC4-2 Hardware Description

2.1 Product Description

The INTERBUS master board IBS USC4-2 integrates all INTERBUS-specific components on a 50 x 70 mm^2 printed circuit board and has an interface to an external dual-port memory (DPM).

In addition to the dual-port memory, the IBS USC4-2 can be extended by a slave interface. This creates an intelligent INTERBUS submaster (system coupler), which works as a slave in a higher-level INTERBUS network and independently operates a lower-level INTERBUS network.

The firmware integrated on the IBS USC4-2 performs all tasks relating to network management and network diagnostics. The firmware operates under a realtime multitasking operating system on sophisticated hardware. A PLC runtime system is also integrated in the firmware and can be used to preprocess process data independently of the host system.

Depending on the requirements of the particular application, the functions of the IBS USC4-2 can be adapted using the appropriate hardware extensions on the carrier board. The structure of the firmware means that various hardware extensions can be supported.

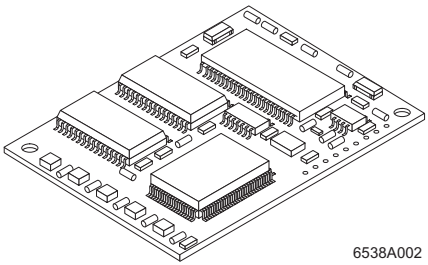


Figure 2-1 Top view of the IBS USC4-2

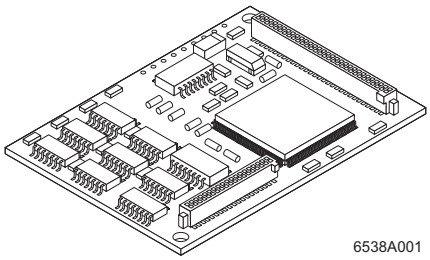


Figure 2-2 Bottom view of the IBS USC4-2

2.1.1 Features

INTERBUS Protocol According to EN 50254

– Master interface and slave interface, as well as extension

Master Interface

Table 2-1 Supported system features depending on the coupling memory

Supports	With a DPM as the Coupling Memory With		
	2 kbytes	4 kbytes	8 kbytes
Maximum number of slave devices (254 remote bus devices/bus segments)	256	512	512
Maximum number of inputs	2048	4096	8192
Maximum number of outputs	2048	4096	8192

– Physical and logical addressing of all slave devices
– Tree structure with up to 16 hierarchical remote bus levels
– Direct data transfer possible without host system participation
– PCP 2.0 (supports parameter channel width of 1, 2 and 4 words), 62/127 (basic functions/maximum extension) devices

Slave Interface

– Supports PCP 2.0
– PCP channel 1, 2 or 4 words
– Process data channel (up to 20 bytes)
– Width of the parameter data and process data channel can be configured from the higher-level INTERBUS network
– Supports program downloads from the higher-level INTERBUS network

Diagnostics via

– On-board LEDs (Section 2.6.6)
– DPM (Section 3)
– Asynchronous serial interface (V.24) (Section 2.6.5)
– Synchronous serial interface (Section 2.6.6)

Interface to the Carrier Board

- 60-pos. SMT female connector
- 40-pos. SMT female connector
- Contains
  - Interface to a dual-port memory (host interface)
  - Interface to IBS SUPI 3 protocol chip and IBS SRE 1 register expansion (slave interface)
  - INTERBUS master interface (CMOS level)
  - Synchronous serial interface (for diagnostic purposes)
  - Asynchronous serial interface (for diagnostics via IBS CMD and firmware updates)
  - In-system programming interface (ISPI) for lattice PLDs
  - 16 MHz clock output (unbuffered)
  - Chip select signals for off-board FLASH blocks for storing configuration data
  - User-defined command sequences (signal interface)
  - Several configuration frames
  - Non-volatile diagnostic data

DPM

- Volatile storage of up to 1024 bytes of input and output data
- 2 mailboxes for the system control panel
- Status/diagnostic area for quick diagnostics

2.1.2 General

The IBS USC4-2 contains all the hardware components that are required for the core of an INTERBUS master. Both master and system coupler functions are supported. Figure 2-3 shows an example INTERBUS network with both functions.

An INTERBUS master has a remote bus interface to the INTERBUS devices and an interface to the relevant host system (e.g., PLC, IPC). Adding a slave interface to the master (e.g., IBS SUPI 3 protocol chip) creates a system coupler.

A system coupler has the same interfaces to INTERBUS and the host system like an INTERBUS master. Like an INTERBUS master, it operates an INTERBUS network independently, but can also exchange data with a hierarchically higher-level INTERBUS network using its slave interface.

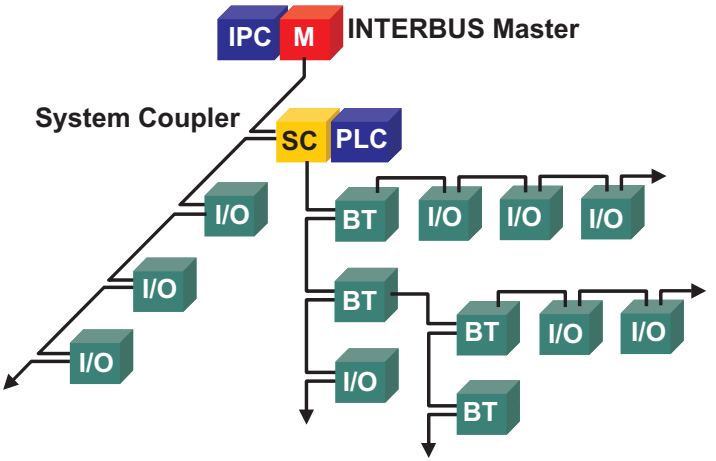


Figure 2-3 Example for an INTERBUS network

To achieve fast response times (2 INTERBUS cycles, maximum), process data can be preprocessed using the IBS USC4-2. In this process, inputs are logically linked and the result is directly transmitted to the outputs. This function is implemented by an algorithm defined by the user using the IBS CMD software. The algorithm is processed by a PLC runtime system. The PLC runtime system is integrated in the IBS USC4-2 firmware.

Table 2-2 provides a brief overview of the performance of the PLC runtime system.

Table 2-2 Performance of the PLC runtime system (processor clock 19.923 MHz)

Instruction	Time (T_{PLC})	Required Memory
1k word instructions	0.7 ms	7 kbytes
1k bit instructions	1.5 ms	15 kbytes

The INTERBUS cycle time increases according to the processing time for the PLC runtime system ($T = T_{Cycle} + T_{PLC}$).

The INTERBUS cycle time is calculated as follows:

$T_{Cycle} = (15 * (8 + n) + 3 * A) * T_{Bit} + T_{SW} + 2 * T_M$

Where

n	Number of bytes of all active field devices in the configuration frame
A	Number of active devices
T_{Bit}	Bit duration (0.002 ms)
T_{SW}	Firmware runtime (0.7 ms)
T_M	Signal runtime on the transmission medium (0.016 ms * km^{-1} for copper)

The value T_{SW} is valid for the physical addressing of the process data. It does not include the time required for logical addressing. To determine the cycle time, a period of 5 µs per logically addressed process data object should be added.

2.2 Mechanics

The dimensions for the six-layer printed circuit board are 50 x 70 mm^2. The board is equipped on both sides. The interfaces of the IBS USC4-2 can be accessed via two SMT female connectors. These are a 60-pos. basic connector and a 40-pos. extension connector. Table 2-3 lists the manufacturer designations for the two female connectors.

Table 2-3 Manufacturer designations for the connectors

Connection	Manufacturer Designation	Manufacturer
60-pos. basic connector	SFM 130 02 FDA	Samtec Europe Ltd.
	SFM 130 02 SDA	Samtec Europe Ltd.
	87023-630	Berg Electronics GmbH
40-pos. extension connector	SFM 120 02 FDA	Samtec Europe Ltd.
	SFM 120 02 SDA	Samtec Europe Ltd.
	87023-620	Berg Electronics GmbH

The signals that can be accessed via the basic connector can be used to operate the IBS USC4-2 with its basic functions. The signals on the extension connector are provided for connecting hardware extensions. Additional information can be found in Sections 2.4 and 2.5.

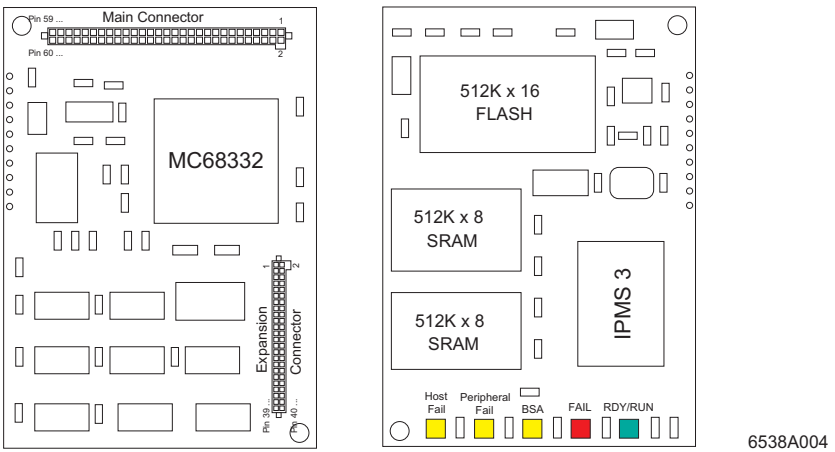


Figure 2-4 Component mounting diagram of the IBS USC4-2

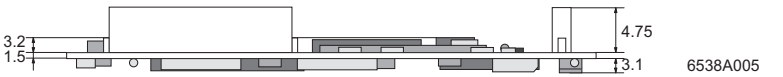


Figure 2-5 Side view of the IBS USC4-2

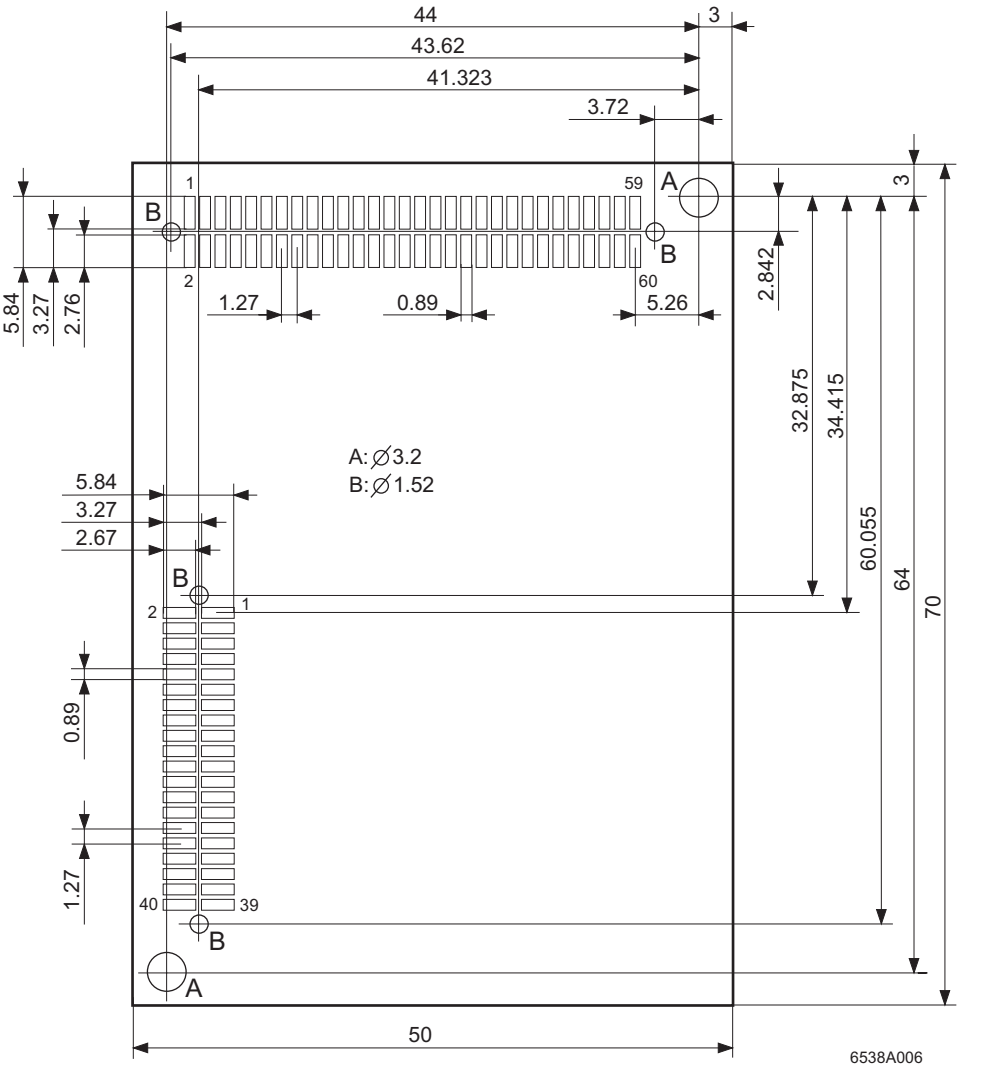


Figure 2-6 Recommended layout of the carrier printed circuit board

2.3 Hardware Structure

Figure 2-7 shows the block diagram of the IBS USC4-2 master board. The individual signals are described on the following pages.

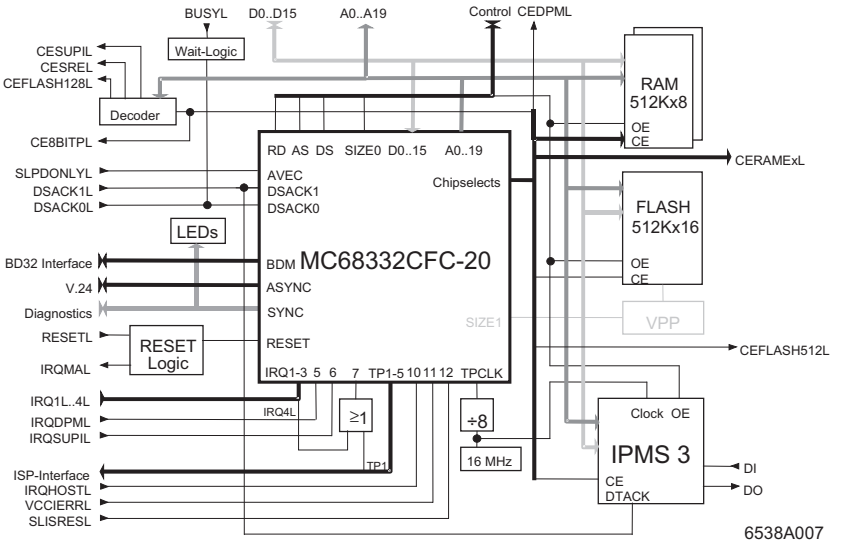


Figure 2-7 Block diagram of the IBS USC4-2

The central unit of the IBS USC4-2 is the Motorola MC68332 microcontroller. It integrates a large part of the necessary I/O devices, such as synchronous and asynchronous serial interfaces, an intelligent 16-channel timer (TPU), a PLL for generating the system clock, and the System Integration Module (SIM) for decoding addresses and generating selection signals. A 1024-kbyte static RAM is provided as the main memory for the microcontroller. Other important components are the word-oriented FLASH memory with a capacity of 1 Mbyte and the INTERBUS master protocol chip IPMS 3.

These components enable the basic functions of the IBS USC4-2. As shown in Figure 2-7, selection signals for the optional hardware extensions are also generated.

Table 2-4 provides an overview of the possible function extensions and the necessary external hardware components. The recommended standard configuration (required by the standard IBS USC4-2 firmware) is indicated by text and fields in bold.

Table 2-4 Function extensions

Hardware Extension	Max. I/Os	Max. Slave Devices	Max. PCP Devices	Non-volatile Parameterization	System Coupler	Memory for PDP
No external RAM	–	–	–	–	–	50 kbytes
1 Mbyte RAM	–	–	–	–	–	50 kbytes
8 kbytes DPM	8192	512	127	–	–	–
2 kbytes DPM	2048	512	32	–	–	–
4 kbytes DPM	**4096**	**512**	**62**	–	–	–
512 kbytes FLASH	–	–	–	**Yes**	–	–
IBS SUPI 3 (+ IBS SRE 1)	–	–	–	–	Yes	–

Key:

PDP Process data preprocessing

Bold Standard hardware configuration

The clock for the IPMS3 INTERBUS master protocol chip (16 MHz) is also used for the TPU of the MC68332.

Some TPU channels are used as status or interrupt inputs. Interrupts can be generated with a rising or falling edge (or both). TPU channels 2, 3, 4 and 5 are used for the ISP interface for programming lattice PLDs (Section 2.6.9).

Some signals (IRQ1L..4L, IRQDPML, IRQSUPIL) are directly linked with the interrupt inputs on the MC68332 to ensure appropriate prioritization. If a multi-port memory (MPM) is used as the coupling memory, inputs IRQ1L to IRQ4L are operated by the MPM logic. All interrupt inputs are fitted with pull-up resistors which means that they do not need to be connected if a dual-port memory (DPM) is used. Conversely, if an MPM is used, the IRGDPML input can remain open.

The RESET logic divides the bi-directional RESET signal of the MC68332 into an input signal (RESETL) and an output signal (SRQMAL). The operating principle is shown in Figure 2-8 and Figure 2-9.

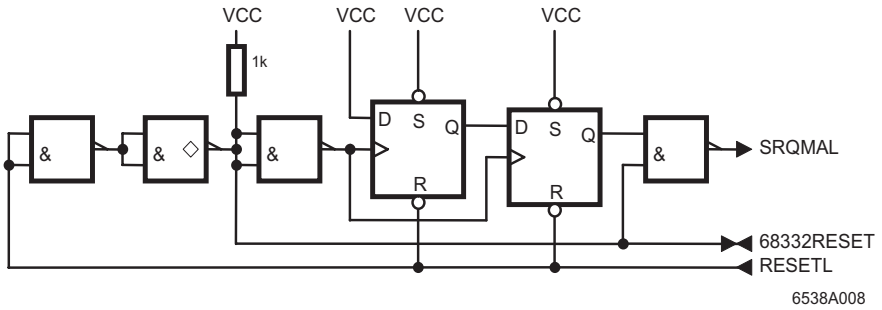


Figure 2-8 RESET logic

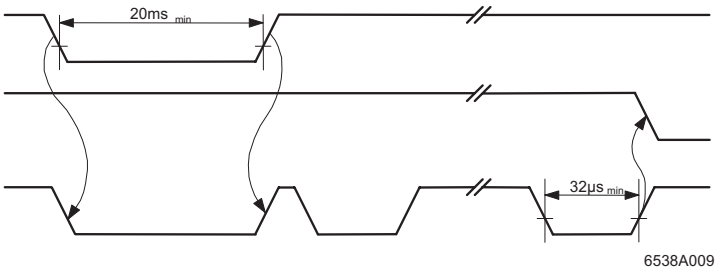


Figure 2-9 RESET timing

The diagnostic indicators are controlled using the synchronous serial interface. On-board diagnostics comprises five LEDs. Additional LEDs or the IBS USC/4-DIAG-L LC display (Order No. 27 46 38 8) can be connected to adapt the diagnostic options to meet the requirements.

The IBS USC4-2 has special selection signals for connecting byte-oriented hardware extensions. These extensions are the protocol chips for the system coupler functionality (IBS SUPI 3, IBS SRE 1). Decoded selection signals are already available for these extensions (CESUPIL, CESREL). Another signal (CE8BITPL), which is not decoded, is reserved for future extensions. This signal must not be used together with the previously decoded signals.

The wait logic on the IBS USC4-2 enables direct connection of byte-oriented standard DPMs.

2.4 Signal Table

Table 2-5 and Table 2-6 list the signals on the IBS USC4-2 connectors with names and pin numbers. The signal direction is given in the "I/O" column.

Table 2-5 Pin assignment of the basic connector

Pin	Signal	I/O	Pin	Signal	I/O
1	VCC	–	31	RDL	CO
2	VCC	–	32	WRL	CO
3	GND	–	33	CEDPML	CO
4	GND	–	34	BUSYL	CI
5	A0	CO	35	CESUPIL	CO
6	A1	CO	36	IRQSUPIL	CI
7	A2	CO	37	Reserved	–
8	A3	CO	38	Reserved	CO
9	A4	CO	39	Reserved	–
10	A5	CO	40	PCS2	CO
11	A6	CO	41	PCS3	CO
12	A7	CO	42	SCK	CO
13	A8	CO	43	MOSI	CO
14	A9	CO	44	MISO	CI
15	A10	CO	45	DO	CO
16	A11	CO	46	DI	CI
17	A12	CO	47	SLISRESL	CI
18	A13	CO	48	RxD	CI
19	A14	CO	49	TxD	CO
20	A15	CO	50	RTS	CO
21	A16	CO	51	CTS	CI
22	D8	CB	52	SRQMAL	CO
23	D9	CB	53	IRQDPML	CI
24	D10	CB	54	IRQHOSTL	CI
25	D11	CB	55	GND	–
26	D12	CB	56	16 MHz clock	CO
27	D13	CB	57	GND	–
28	D14	CB	58	Reserved	CI
29	D15	CB	59	VCC	–
30	RESETL	CI	60	VCC	–

CO: CMOS output; CI: CMOS input; CB: CMOS bi-directional

Table 2-6 Pin assignment of the extension connector

Pin	Signal	I/O	Pin	Signal	I/O
1	D0	CB	21	ISPSDOUT	CI
2	D1	CB	22	LMODE	CI
3	D2	CB	23	CERAMEUL	CO
4	D3	CB	24	CERAMELL	CO
5	D4	CB	25	CESREL	CO
6	D5	CB	26	CEFLASH512L	CO
7	D6	CB	27	IRQ1L	CI
8	D7	CB	28	IRQ2L	CI
9	A17	CO	29	IRQ3L	CI
10	A18	CO	30	IRQ4L	CI
11	A19	CO	31	DSACK0L	CI
12	ASL	CO	32	DSACK1L	CI
13	DSL	CO	33	VCCIERRL	CI
14	RHWL	CO	34	BD32VPP	–
15	SIZEBHWL	CO	35	BD32RPL	–
16	ISPSDIN	CO	36	BD32IPIPE	CB
17	ISPSCLK	CO	37	BD32IFETCH	CB
18	ISPMODE	CO	38	BD32MARESL	CB
19	ISPENL	CO	39	BD32FREEZE	CB
20	CE8BITPL	CO	40	BD32BKPT	CI

CO: CMOS output; CI: CMOS input; CB: CMOS bi-directional

2.5 Signal Description

Table 2-7 Signal description

Signal(s)	Description
A0...A19	Address bus; contains the byte (or high-order byte) address that is transmitted over the data bus. A19 is the most significant address bit.
ASL	Active-low address strobe; this signal is active if the address bus contains a valid address.
BD32BKPT BD32FREEZE BD32IFETCH BD32IPIPE BD32MARESL BD32RPL BD32VPP	These signals are part of the Background Debug Mode Interface (BDMI) of the IBS USC4-2. Further information can be found in the Motorola "MC68332 User's Manual". For write access to the optional parameterization memory signal BD32VPP is switched to 12 V. In idle state, this signal carries 5 V. The signal is used for INTEL-compatible flash types.
BUSYL	Active-low input signal controlled by the DPM. It is active when there is an address conflict upon access to a DPM. The signal is evaluated and processed by the internal wait logic of the IBS USC4-2. If a multi-port memory (MPM) or a word-oriented DPM is used as the coupling memory, this input must be connected to GND to disable the wait logic of the IBS USC4-2. When using an MPM, access control is also carried out by the MPM. When using a word-oriented DPM, an external wait logic has to be implemented. It is described under "Dual-Port Memory (DPM)" on page 2-18.
CE8BITPL	Active-low selection signal for byte-oriented I/O components. Unlike the CESUPIL and CESREL signals, this signal is not decoded and is therefore active in the entire address areas for byte-oriented I/O components. It must not be used together with the signals listed above.
CEDPML	Active-low selection signal for the dual-port memory (DPM). The IBS USC4-2 activates this signal when the DPM is accessed.
CEFLASH512L	Active-low selection signal for the optional 512-kbyte FLASH block (parameterization memory). The IBS USC4-2 activates this signal when this FLASH block is accessed.
CERAMELL CERAMEUL	Active-low selection signal for the external RAM extension. Two selection signals are provided to enable separate access to the high-order and low-order byte of a word operand. CERAMELL is activated when the low-order byte (bits 0...7) is accessed; CERAMEUL is activated when the high-order byte (bits 8...15) is accessed.
CESREL	Active-low selection signal for the IBS SRE 1 register expansion chip in the optional INTERBUS slave interface. The IBS USC4-2 activates this signal when the IBS SRE 1 is accessed.

Table 2-7 Signal description

Signal(s)	Description
CESUPIL	Active-low selection signal for the byte-oriented block in the optional INTERBUS slave interface. If only the basic connector signals are used, this signal must be further decoded to generate separate selection signals for the INTERBUS IBS IBS SUPI 3 slave protocol chip and the IBS SRE 1 register expansion. The IBS USC4-2 activates this signal when the blocks in the optional INTERBUS slave interface are accessed.
CTS, RTS RxD, TxD	Signals TxD, RxD, CTS and RTS are part of the asynchronous serial interface on the IBS USC4-2. RxD and CTS are CMOS inputs, TxD and RTS are CMOS outputs.
D0...D15	Bi-directional data bus; contains the data to be transmitted to or from the IBS USC4-2. Byte-oriented devices must be connected to D8...D15.
DI DO	Data signals for INTERBUS. DI is a CMOS input and DO is a CMOS output. Electrical isolation and conversion to the necessary physical INTERBUS transmission method (e.g., RS422, fiber optics) are carried out outside the IBS USC4-2.
DSACK0L DSACK1L	These active-low input signals enable asynchronous data transfer with dynamic adaptation of the data bus width between the IBS USC4-2 and the coupling memory.
DSL	Active-low output signal. The IBS USC4-2 activates this signal on a read cycle to indicate that the selected I/O component should place valid data on the data bus. Activation of this signal on a write cycle means that valid data is available on the data bus.
GND	Connects the power supply GND to the IBS USC4-2. Several pins are connected to GND to ensure the current carrying capacity. All power supply connections must be used.
IRQ1L IRQ2L IRQ3L IRQ4L	Active-low input signals for MPM interrupt requests. If a DPM is used as the coupling memory, these inputs may remain unconnected.
IRQDPML	Active-low input signal for DPM interrupt requests. It is activated on a DPM interrupt request.
IRQHOSTL	Active-low input signal. Activation of this signal informs the IBS USC4-2 about a serious malfunction in the host system. This resets all INTERBUS outputs. In addition, the "HF" LED indicates the status of this signal (LED is on if IRQHOSTL is active).

Table 2-7 Signal description

Signal(s)	Description
IRQSUPIL	Active-low input signal for interrupt requests of the IBS SUPI 3 INTERBUS slave protocol chip in the optional INTERBUS slave interface. It is activated on a IBS SUPI 3 interrupt request.
ISPENL ISPMODE ISPSCLK ISPSDIN ISPSDOUT	These signals enable lattice PLDs to be programmed by the IBS USC4-2. They can be directly connected to the corresponding SDIN, SDOUT, SCLK, MODE and ISPEN pins on the system programming interfaces (ISP) of the lattice PLDs. If these signals are not used, these pins can remain unconnected.
LMODE	This active-high input signal can be used to activate "learn mode", for example, by pressing a button on the diagnostic LDC. The status of this signal is evaluated after the IBS USC4-2 self test has been completed. If the signal is active (button pressed), the currently connected INTERBUS configuration is read automatically and stored in the optional parameterization memory. The INTERBUS devices are physically addressed and data transmission is started. If no INTERBUS devices are connected, all parameterization data previously stored in the optional parameterization memory is deleted.
MISO MOSI PCS2 PCS3 SCK	These signals are part of the synchronous serial interface of the MC68332. They are used to connect additional diagnostic equipment. Except for MISO, all signals are CMOS outputs. MISO (master in slave out) is a CMOS input.
RDL	This active-low output signal is activated by the IBS USC4-2 on a read cycle.
RESETL	This active-low input signal is controlled by an external reset logic. Activating this signal resets the IBS USC4-2.
RHWL	This output signal is used by the IBS USC4-2 to indicate the direction of data transmission. A high level indicates read access; a low level indicates write access.
SIZEBHWL	This output signal is used by the IBS USC4-2 to indicate the size of the operand to be transmitted. A high level indicates transmission of a byte operand; a low level indicates transmission of a 2-byte or word operand.
SLISRESL	This active-low input signal is controlled by the optional INTERBUS slave interface. It is activated when the INTERBUS slave interface is in the RESET state.
SRQMAL	In the event of a serious malfunction on the IBS USC4-2 (e.g., defective quartz, software watchdog triggered), this active-low signal is activated.

Table 2-7 Signal description

Signal(s)	Description
VCC	Connects the power supply to the IBS USC4-2. Several pins are connected to VCC to ensure the current carrying capacity. All power supply connections must be used.
VCCIERRL	This active-low input signal can be used to report the failure of the supply voltage for the electrically isolated RS485 interface to the IBS USC4-2. The signal is generated by a voltage monitoring circuitry within the electrically isolated area.
WRL	This active-low output signal is activated by the IBS USC4-2 on a write cycle.
16 MHz clock	A clock signal with a frequency of 16 MHz is available at this output. If this clock is used for external purposes, the signal must be buffered or filtered directly at the basic connector in order to avoid disturbing affects due to overload or electromagnetic interference.

Further information on the MC68332 features can be found in the Motorola "MC68332 User's Manual".

2.6 Extension Options

Figure 2-10 shows the IBS USC4-2 with all its supported extensions. Figure 2-11 shows an overview of the structure of an INTERBUS master and an INTERBUS system coupler.

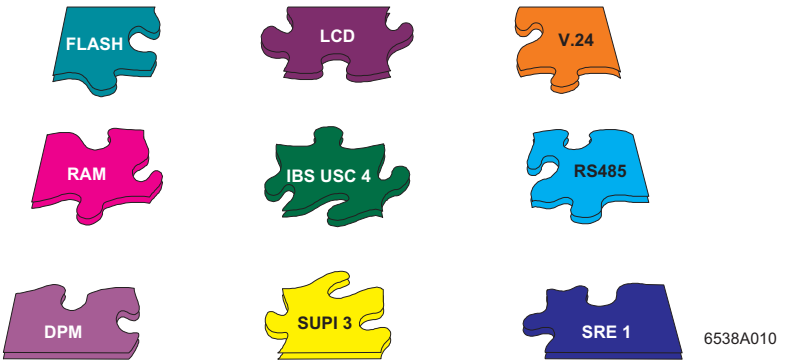


Figure 2-10 IBS USC4-2 and supported hardware extensions

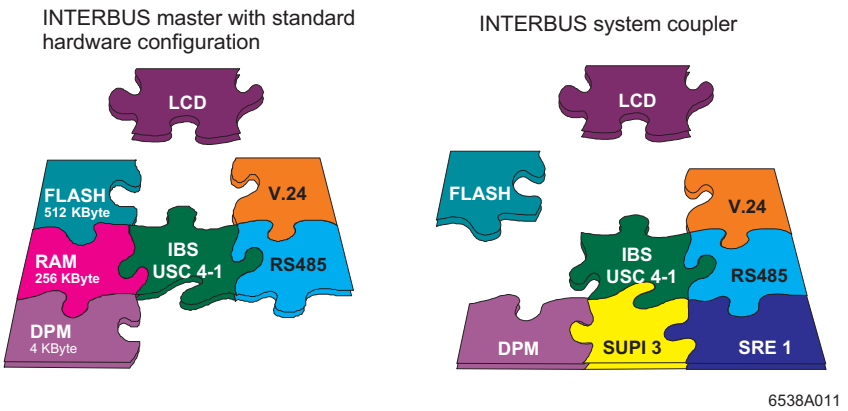


Figure 2-11 Hardware configuration examples

Like the predecessor IBS USC4-1, the IBS USC4-2 is delivered with a standard firmware. The standard firmware is designed for a configuration, which can be used in almost all implementations (Figure 2-11).

In the event of deviations from the standard configuration, the IBS USC4-2 must be reconfigured via the BD32 interface. Each part of the puzzle stands for a more or less complex hardware structure, which is described on the following pages.

2.6.1 Dual-Port Memory (DPM)

The DPM is used as the coupling memory between the IBS USC4-2 and the relevant host system. The size of the DPM determines, for example, the number of I/O points that can be connected. Figure 2-12 and Figure 2-14 show the connection of different DPMs to the IBS USC4-2.

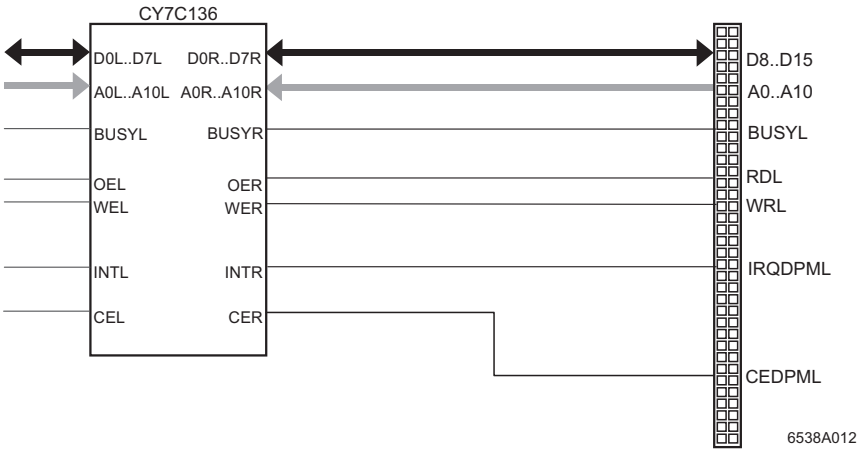


Figure 2-12 Connection of the 2k x 8 DPM

If more than 2048 binary inputs and outputs are to be processed, an additional 2k x 8 DPM must be implemented. The data bus width also is 8 bits.

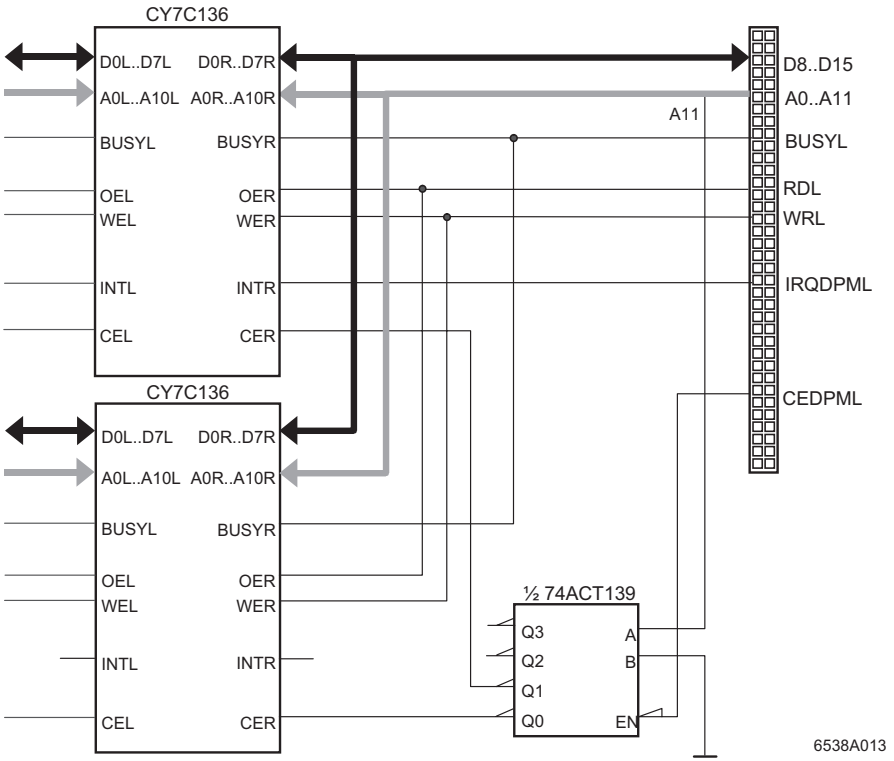


Figure 2-13 Connection of two 2k x 8 DPMs

Implementing an 8-kbyte DPM is required to support more than 4096 inputs/outputs in the INTERBUS system. Using firmware version 4.6 and later this configuration manages up to 8192 inputs/outputs. Wiring of the 8-kbyte (4k x 16) DPM is shown in Figure 2-14.

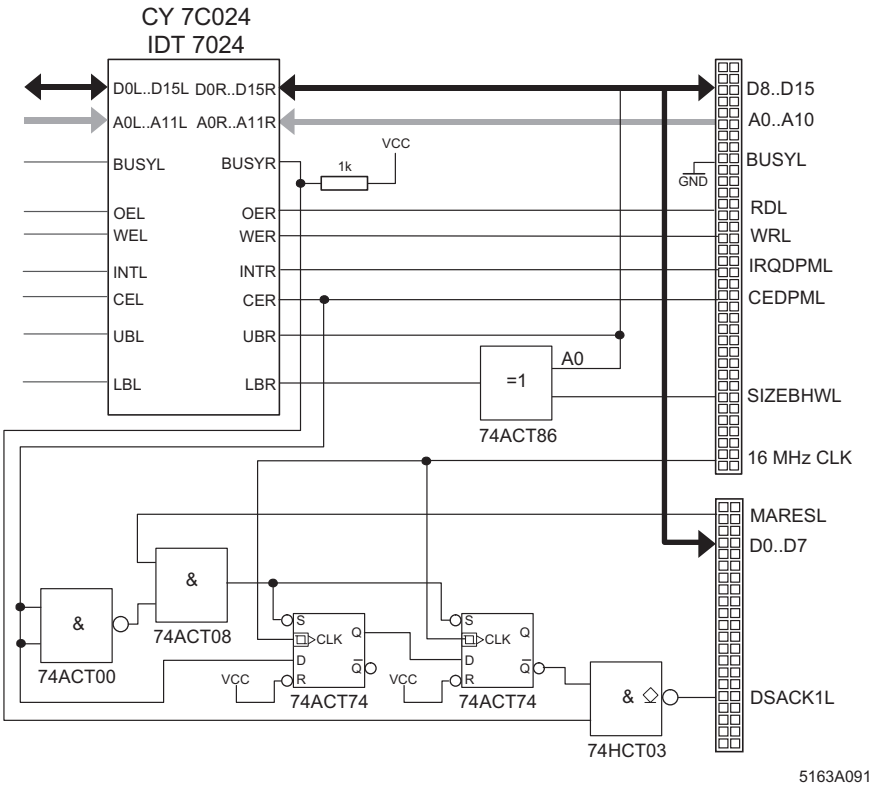


Figure 2-14 Connection of a 4k x 16 DPM

Table 2-8 shows a list of all the supported DPM blocks.

Table 2-8 Supported DPM blocks

Manufacturer	Manufacturer Designation	Memory Capacity
Cypress	CY7C136	2 kbytes
IDT	IDT 71321	2 kbytes
Cypress	CY7C024-35 AC	8 kbytes
Cypress	CY7C024-35 AI	8 kbytes
Cypress	CY7C024-15 AI	8 kbytes
Cypress	CY7C024-15 AC	8 kbytes
IDT	IDT 7024 S 35 PF	8 kbytes
IDT	IDT 7024 S 15 PF	8 kbytes
IDT	IDT 7024 S 15 PFI	8 kbytes

2.6.2 FLASH

The external FLASH memory block is used for non-volatile storage of parameterization data. This includes INTERBUS configuration data, algorithms for process data preprocessing or user-defined command sequences. Figure 2-15 shows the FLASH memory block connected to the IBS USC4-2. Table 2-9 and Table 2-10 list the supported FLASH types.

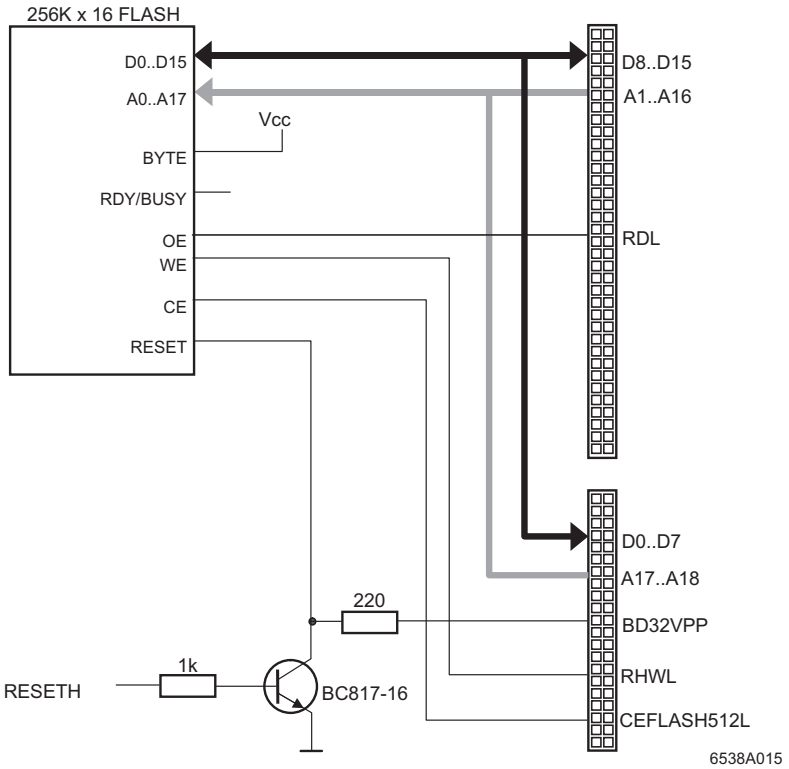


Figure 2-15 Connection of an INTEL-compatible 256k x 16 FLASH memory block

Table 2-9 Supported INTEL-compatible FLASH memory blocks

FLASH	Manufacturer Designation	Manufacturer
256k x 16 / V_{pp} = 12 V	M28F420B	ST Microelectronics
256k x 16 / V_{pp} = 12 V	PA28F400B	INTEL
256k x 16 / V_{pp} = 5 V	AM29F400B	AMD
256k x 16 / V_{pp} = 5 V	M29F400B	ST Microelectronics

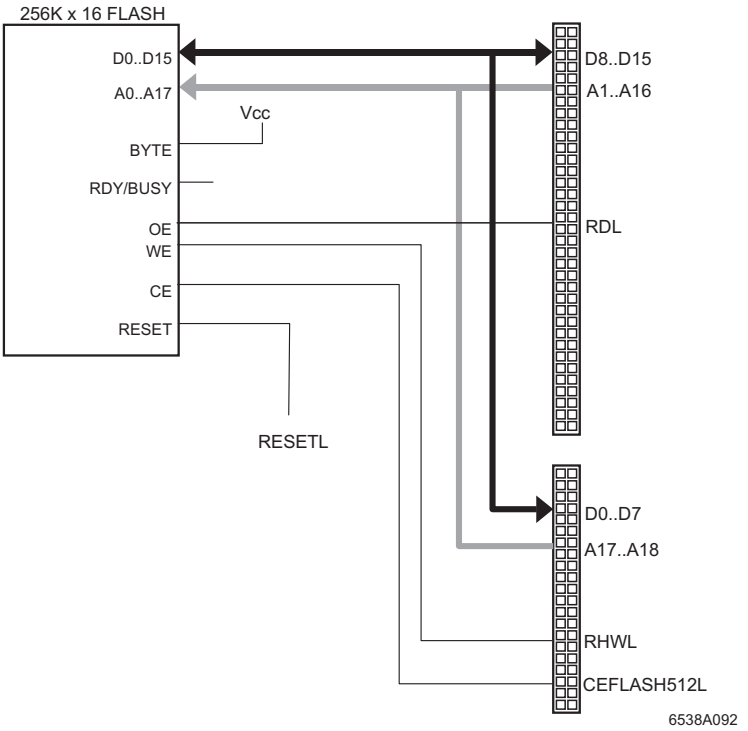


Figure 2-16 Connection of an AMD-compatible 256k x 16 FLASH memory block

Table 2-10 Supported AMD-compatible FLASH memory blocks

FLASH	Manufacturer Designation	Manufacturer
256k x 16	AM29F400 BB-70SC	AMD
256k x 16	AM29F400BB-55SC	AMD
256k x 16	MBM29F400 BC-70PF	Fujitsu Mikroelektronik
256k x 16	MBM29F400 BC-55PF	Fujitsu Mikroelektronik
256k x 16	M29F400 BB70M1T	ST Microelectronics
256k x 16	M29F400 BB55M1T	ST Microelectronics

Please note that pin 1 of the AMD-compatible flash memory block must not be wired!

2.6.3 RAM

Implementation of an external 1-Mbyte RAM extension is optional and provides memory capacities for future requirements. Figure 2-17 illustrates the connection of an external RAM block to the IBS USC4-2. Under normal circumstances, the on-board RAM is sufficient for the current IBS USC4-2 scope of functions.

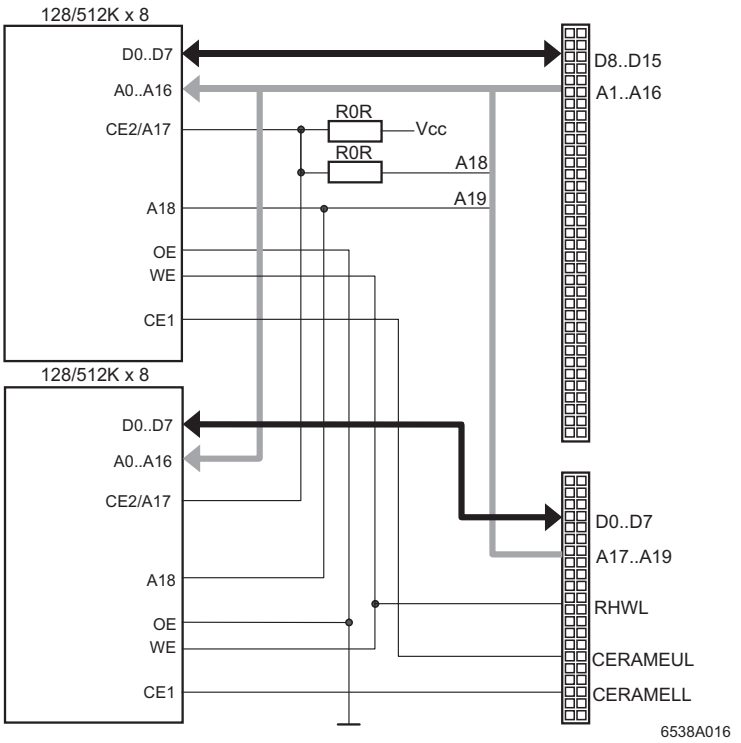


Figure 2-17 Connection of a 1-Mbyte RAM

Table 2-11 Supported RAM blocks

RAM	Manufacturer Designation	Manufacturer
512k x 8	HM 628512 LFP-7	Hitachi
512k x 8	KM 684000 BLG-7L	Samsung
512k x 8	K6T4008C1B-GB70	Samsung
512k x 8	TC 554001 FL-70	Toshiba
512k x 8	TC 554001 FL-70L	Toshiba
512k x 8	TC 554001 AF-70L	Toshiba

2.6.4 INTERBUS Interface

The INTERBUS interface connects the IBS USC4-2 to the INTERBUS network. Table 2-12 shows the pin assignment of the interface designed as an electrically isolated 9-pos. D-SUB female connector for signal transmission using a copper cable. Please contact Phoenix Contact if you want to implement interfaces for other transmission media.

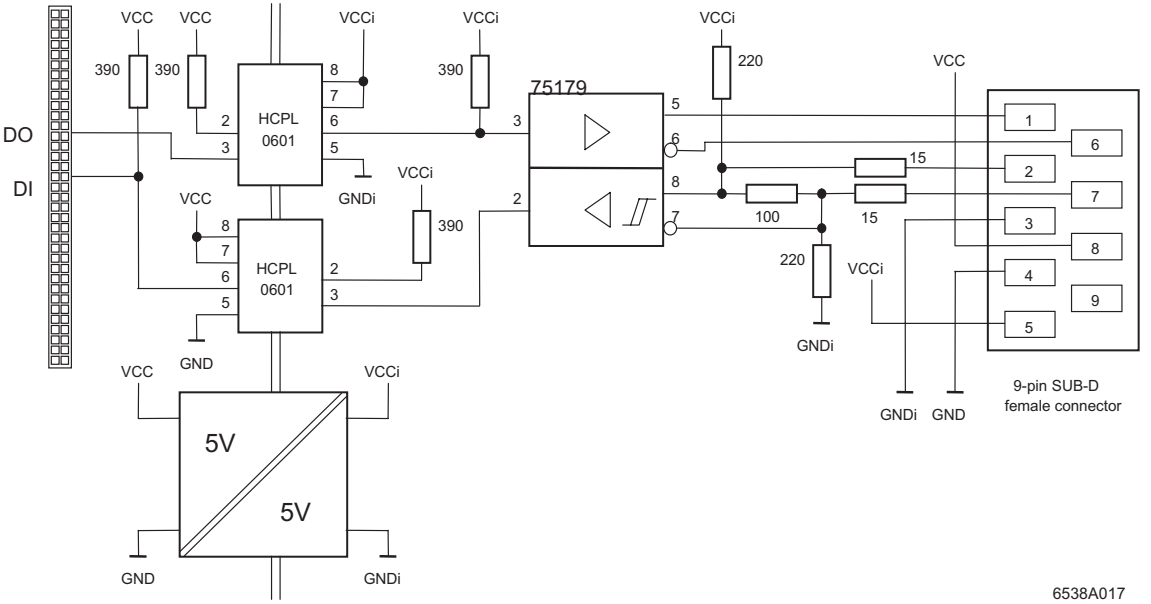


Table 2-12 Pin assignment of the INTERBUS interface

Pin	Signal	Pin	Signal
1	DOH	6	DOL
2	DIH	7	DIL
3	GNDi	8	Vcc
4	GND	9	N.C.
5	Vcci		

Figure 2-18 Connection of the INTERBUS interface (D-SUB9)

Table 2-13 Recommended components for the INTERBUS interface

Component Designation	Manufacturer Designation	Manufacturer
RS485 driver	SN 75179 B DR	TEXAS INSTRUMENTS
Optocoupler	HCPL 0601 OPTION 500	HEWLETT PACKARD
	NTE 0505 M	C&D Technologies
	AME 0505 TM	DORSCH Elektronik
DC/DC converter 5V/5V	1NUS5N5Y	M+R Multitronik
	R05SS05	RECOM Electronic
	RSS-0505	RECOM Electronic
	TSM0505S	TRACO

For additional recommendations on components and the design of an INTERBUS interface, please refer to the latest INTERBUS certification guidelines. They are available for download on the INTERBUS Club homepage www.interbusclub.com).

2.6.5 V.24 Interface

The V.24 interface is available on every INTERBUS master. It is used as a parameterization and diagnostic interface. The master board can be parameterized and operated using different software tools.

IBS CMD SWT G4 E (Order No. 27 21 44 2) is the main software tool for parameterizing and starting up a system. Additional parameterization, like assigning the program addresses to the I/O modules, completes bus configuration in CMD. Monitoring functions and easy handling, e.g., for connecting and disconnecting the bus segments, support the user when testing the functions and setting up the system step-by-step. Data export to the EPLAN E-CAD system replaces the repeated manual entry of data. The bus-related and automatic creation of the circuit diagram (with EPLAN) in line with CMD data drastically reduces documentation times. It is also possible to read back the signal data in CMD. At the same time, CMD generates the relevant assignment lists or imports them into CMD, depending on the control system used.

With the user-friendly diagnostic function integrated in CMD, fast and clear troubleshooting is possible in the event of an error.

Diag+

In addition, the IBS USC4-2 supports the INTERBUS diagnostic tool Diag+ (IBS DIAG+ SWT / Order No. 27 30 30 7). With the universal activeX-compatible Diag+ tool it is now possible to directly integrate the INTERBUS diagnostics tool in other software applications, e.g., process visualization. The development time previously required for creating individual diagnostic interfaces in the visualization system, for programming transfer functions for diagnostic data in the control program, and also for programming evaluation functions for diagnostic data is therefore no longer necessary. Clear text messages and all available status information can be directly accessed by the visualization system or the corresponding activeX container.

For further information on CMD and Diag+, please refer to our homepage www.automation.phoenixcontact.com.

Non-volatile parameterization via the V.24 interface is only possible if the IBS USC4-2 has access to a parameterization memory (FLASH extension). In this case the user-defined parameterization data can be stored in a non-volatile memory. The V.24 interface is a 9-pos. D-SUB connector with the pin assignment shown in Table 2-15.

Table 2-14 Recommended components for the V.24 interface

Manufacturer Designation	Manufacturer
MAX 202 ECSE-T	MAXIM
SP 202 ECN/TR	SIPEX
ADM 202 E	ANALOG Devices

Table 2-15 Pin assignment of the V.24 interface

Pin	Signal
1	N.C.
2	TxD
3	RxD
4	N.C.
5	GND
6	N.C.
7	RTS
8	CTS
9	N.C.

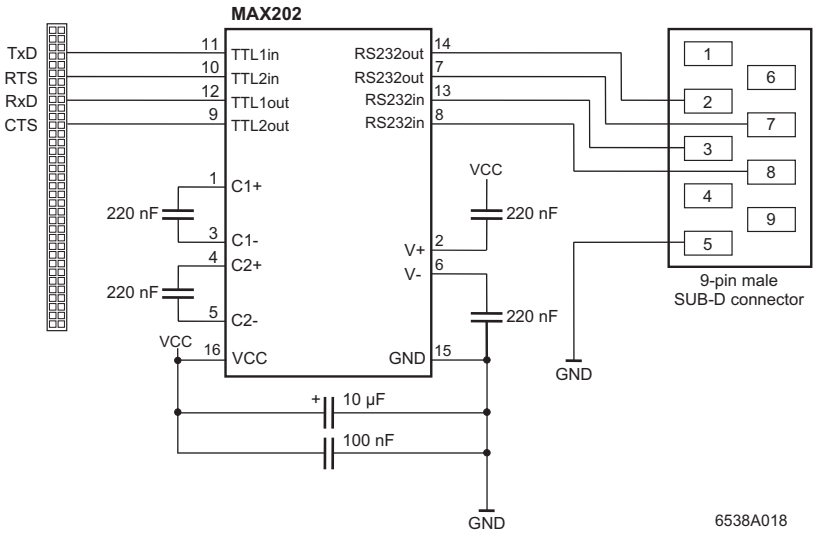


Figure 2-19 Connection of the V.24 interface (example circuit diagram with MAX 202)

2.6.6 Diagnostic Interface

The diagnostic interface on the IBS USC4-2 is used to control additional diagnostic displays outside the IBS USC4-2. In the most simple case, this involves four or five LEDs, which are required for the basic visual diagnostics of the INTERBUS system. The LED indicating a host system failure (HF) can be omitted if the host system itself is fitted with this type of indicator or if it is not required.

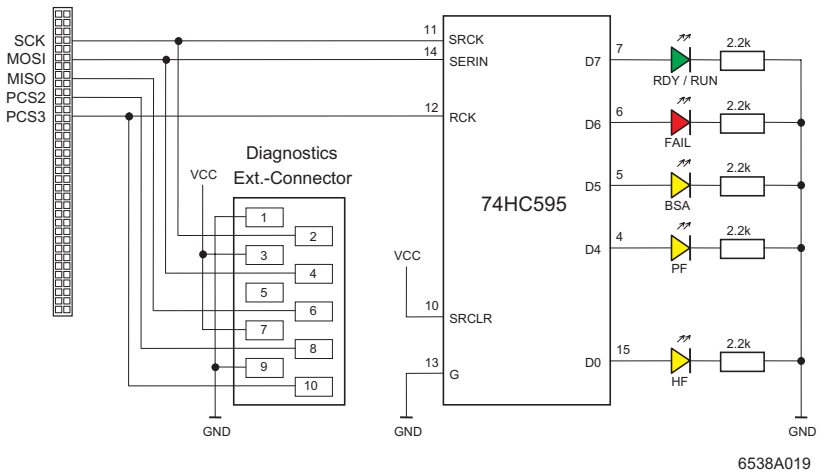


Figure 2-20 Connection of the diagnostic interface with a serial/parallel converter

Figure 2-20 shows the connection of additional diagnostic LEDs. The wiring example also shows the wiring for the diagnostic extension connector. This connector is designed as a 10-pos. plug-type connector and can be used to connect an (optional) diagnostic extension, e.g., IBS USC/4-DIAG-L LC display (Order No. 27 46 38 8).

Table 2-16 Recommended serial/parallel converters for the diagnostic interface

Manufacturer Designation	Manufacturer
74 HC 595 D/T3	PHILIPS
TC 74 HC 595 AFN-ELP	TOSHIBA

Table 2-17 shows an overview of the meanings of the diagnostic LEDs on the IBS USC4-2.

Table 2-17 Diagnostic LEDs

LED	Color	Meaning
RDY/RUN	Green	Flashing: READY / ACTIVE ON: RUN
FAIL	Red	OFF: No error ON: Remote bus, local bus, controller, watchdog or hardware error
BSA	Yellow	ON: Bus segment aborted
PF	Yellow	ON: Peripheral fault
HF	Yellow	ON: Malfunction in host system

Provision of a diagnostic extension connector on the carrier printed circuit board of the IBS USC4-2 is strongly recommended.

2.6.7 INTERBUS Slave Interface

Extending the IBS USC4-2 by an INTERBUS slave interface creates an INTERBUS system coupler. The INTERBUS slave interface in Figure 2-21 has its own power supply so that data transmission in the higher-level INTERBUS network is not interrupted in the event of a master power supply failure or shutdown. Because of the separate power supply of master and slave the signals between these parts must be buffered to prevent an undesirable current flow during operation of only one part.

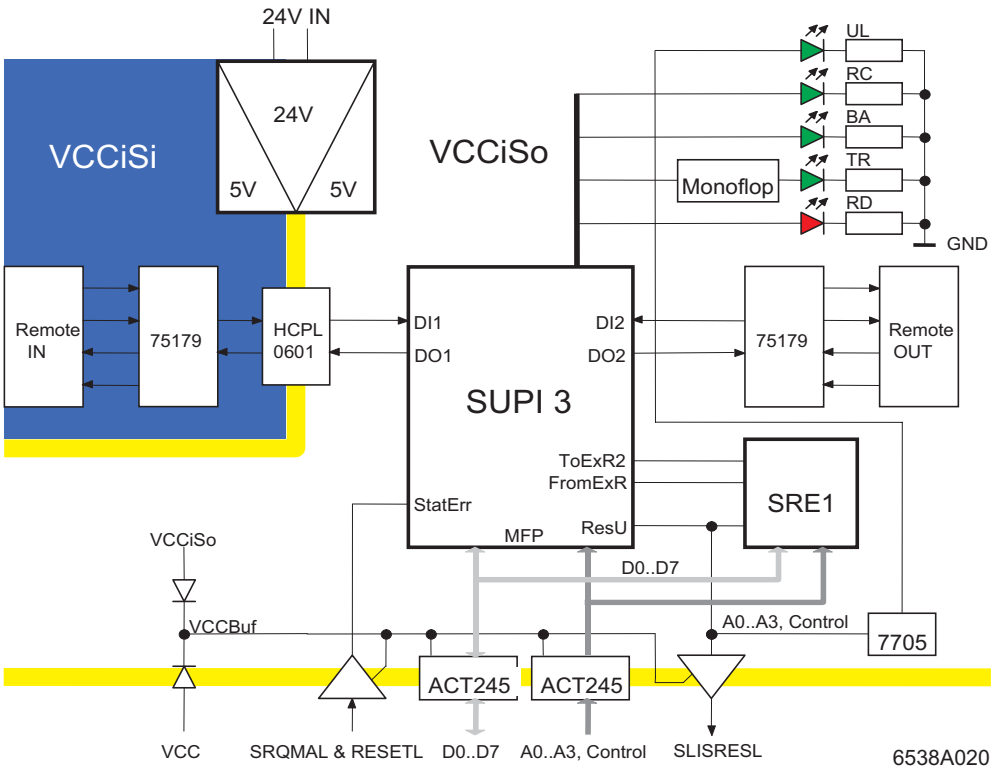


Figure 2-21 Connection of the INTERBUS slave interface

2.6.8 BD32 Interface

The signals of the BD32 interface are shown in Figure 2-22. The BD32 interface signals **must be brought out** onto the carrier printed circuit board of the IBS USC4-2 because the IBS USC4-2 firmware can only be reconfigured using this interface. The IBS USC4-2 is supplied with a standard firmware (Table 2-4 on page 2-9), which is designed for a standard configuration. If the external hardware configuration deviates from the standard, the master board must be reconfigured.

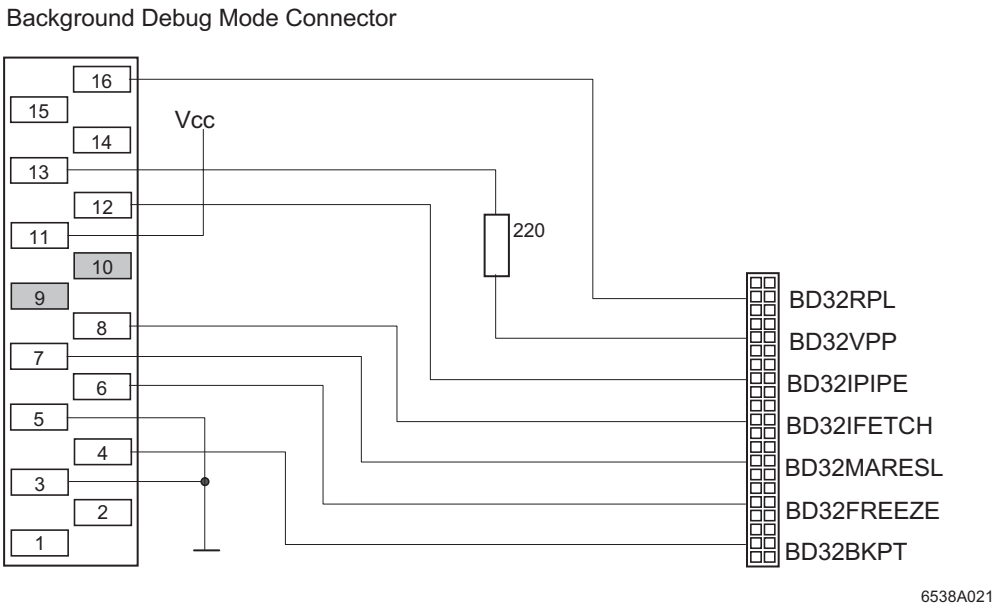


Figure 2-22 Connection of the BD32 interface

Use of this connection on the carrier printed circuit board is **strongly recommended**. If the external hardware components deviate from the standard configuration, the firmware must be reconfigured using the BD32 interface.

2.6.9 ISP Interface

When implementing the host interface (interface between the IBS USC4-2 and the host system), programmable logic devices (PLDs) are used frequently. A special interface, the in-system programming interface (ISPI), is integrated on the IBS USC4-2 for programming lattice PLDs.

This programming interface can be used to program PLDs from the PC using the BD32 adapter. Figure 2-23 shows the connection of lattice PLDs to the ISPI.

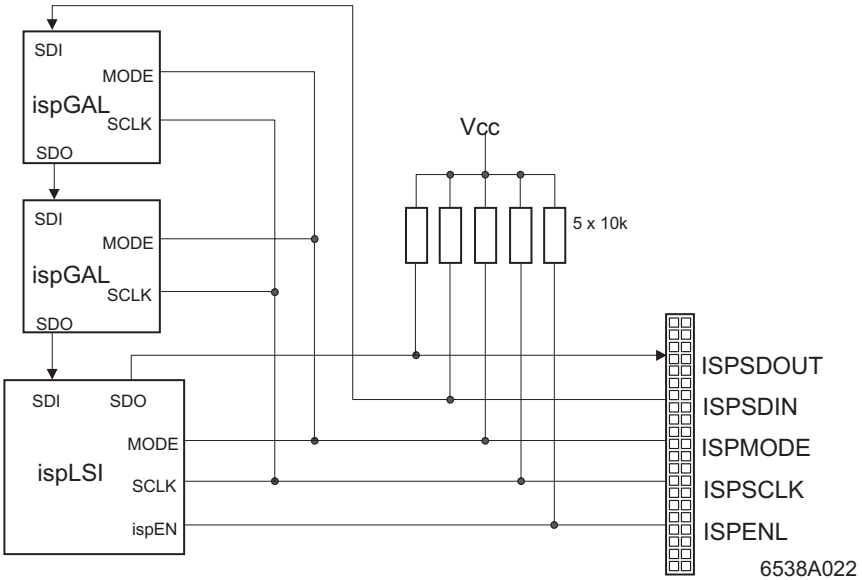


Figure 2-23 Connection of lattice PLDs

2.7 Timing Diagrams

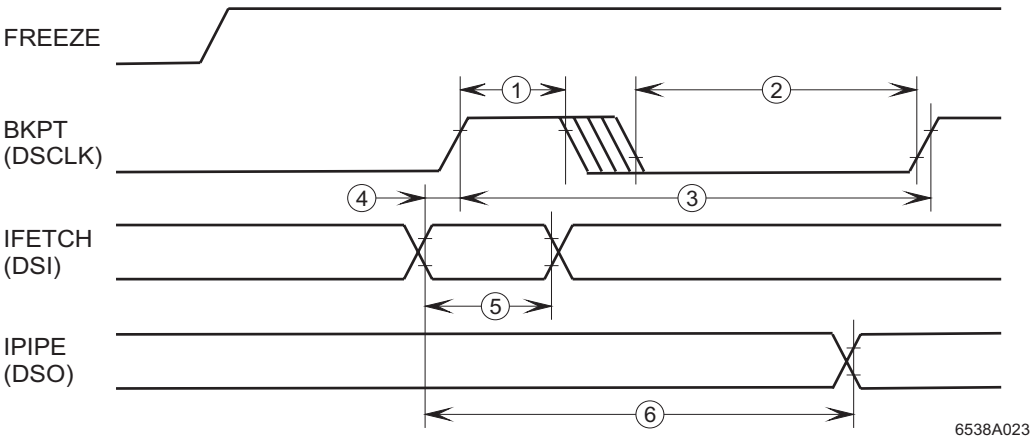


Figure 2-24 Background debug mode - serial communication

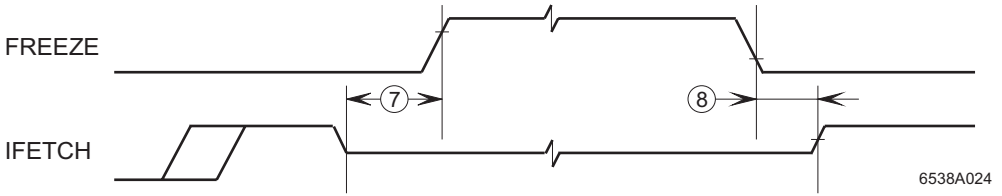


Figure 2-25 Background debug mode - FREEZE activation

Table 2-18 Background debug mode

No.	Characteristic	Min.	Max.	Unit
1	DSCLK high time	85	-	ns
2	DSCLK low time	120	-	ns
3	DSCLK cycle time	205	-	ns
4	DSI valid to DSCLK high (DSI setup)	0	-	ns
5	DSI valid	85	-	ns
6	DSO delay	-	170	ns
7	IFETCH in high impedance to FREEZE asserted	0	-	ns
8	IFETCH valid after FREEZE negated	0	-	ns

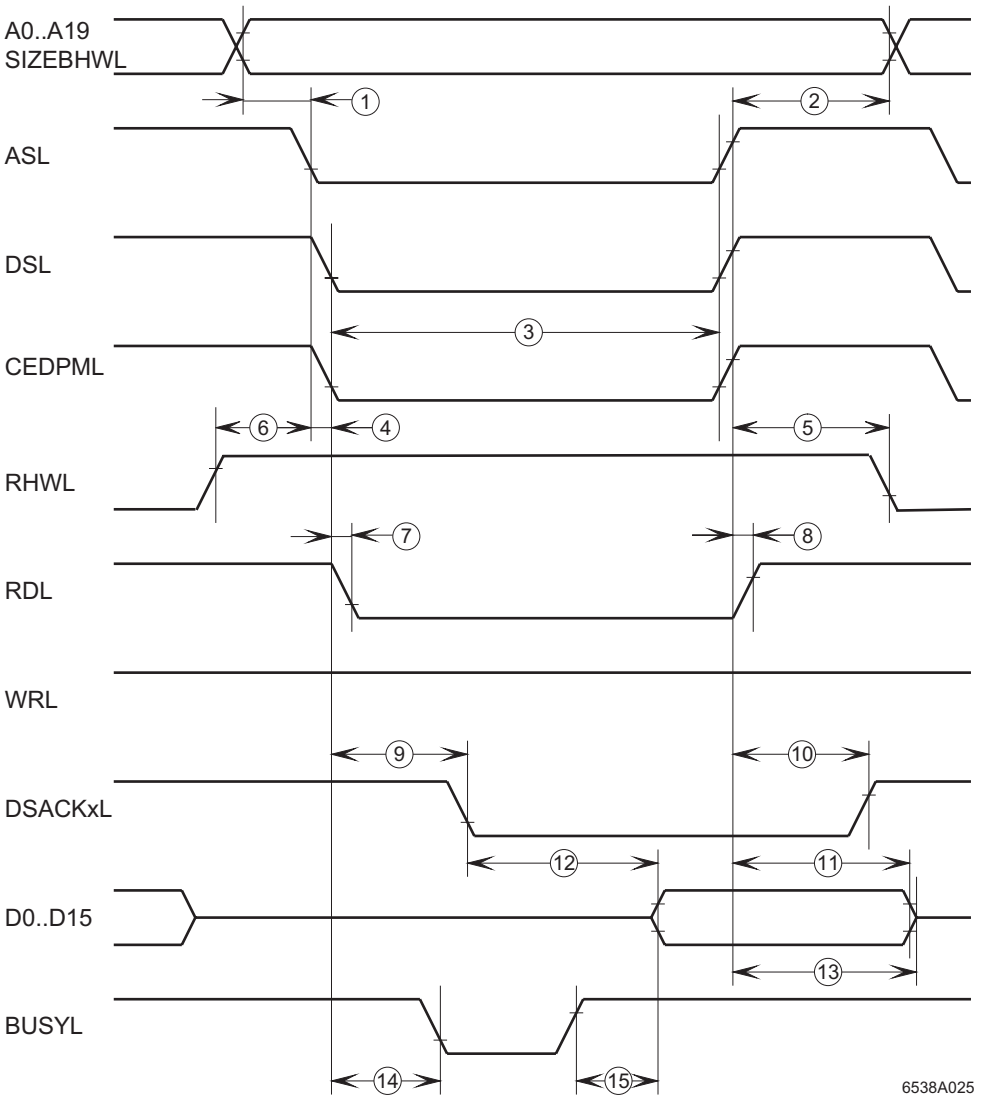


Figure 2-26 DPM/MPM read access

Table 2-19 DPM/MPM read access

No.	Characteristic	Min.	Max.	Unit
1	Address valid to ASL asserted	10	–	ns
2	ASL, DSL, CEDPML negated to address invalid (address hold)	10	–	ns
3	CEDPML width asserted	80	–	ns
4	ASL to DSL or CEDPML asserted	-10	10	ns
5	ASL, DSL, CEDPML negated to RHWL low	10	–	ns
6	RHWL high to ASL asserted	10	–	ns
7	CEDPML asserted to RDL asserted	–	20	ns
8	RDL negated after ASL, DSL, CEDPML negated	1	10	ns
9	CEDPML asserted to DSACKx asserted	0	–	ns
10	DSACKx negated after ASL, DSL, CEDPML negated	0	60	ns
11	DSL, CEDPML negated to data invalid (data hold)	0	–	ns
12	Data valid after DSACKxL asserted	–	46	ns
13	CEDPML negated to data in high impedance	–	48	ns
14	BUSYL asserted after CEDPML asserted	–	75	ns
15	BUSYL negated to data valid	–	56	ns

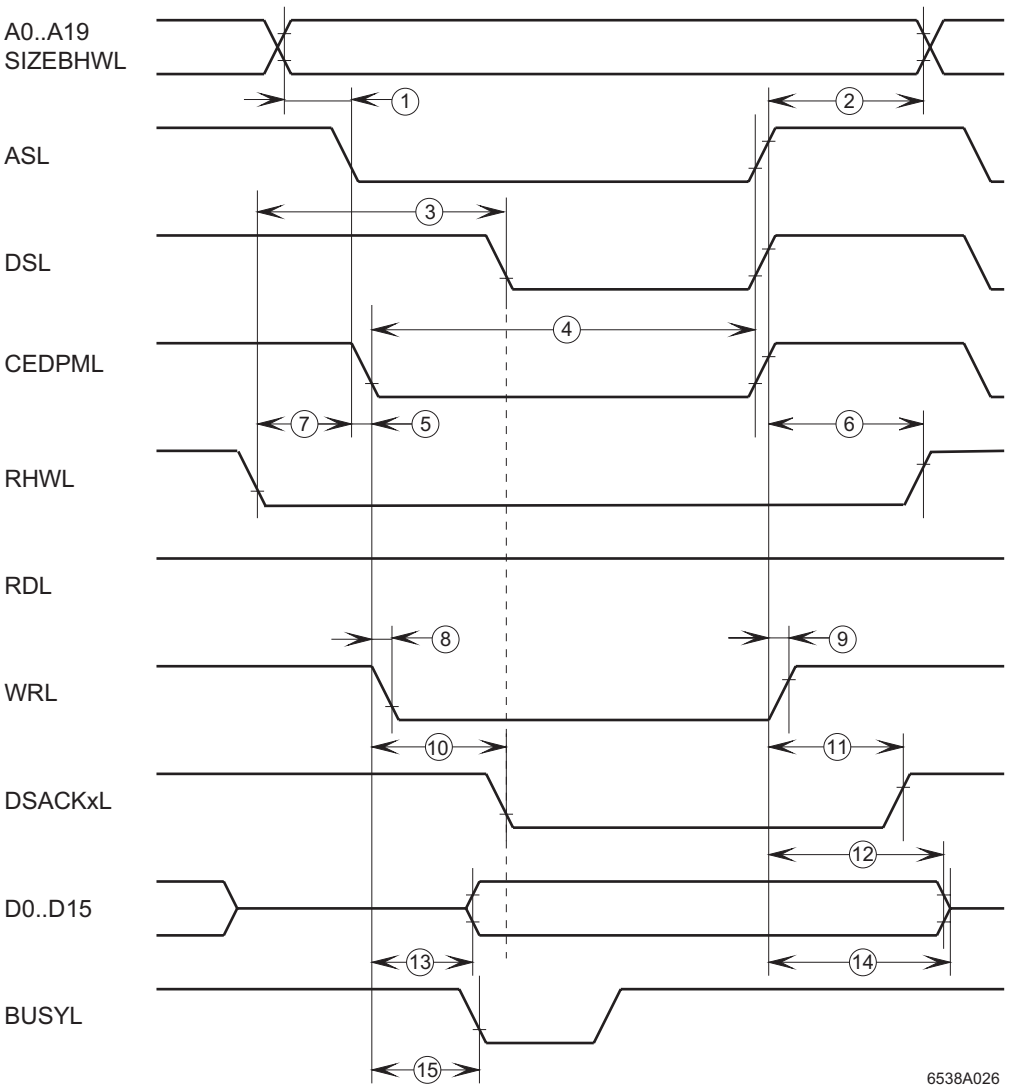


Figure 2-27 DPM/MPM write access

Table 2-20 DPM/MPM write access

No.	Characteristic	Min.	Max.	Unit
1	Address valid to ASL asserted	10	–	ns
2	ASL, DSL, CEDPML negated to address invalid (address hold)	10	–	ns
3	RHWL low to DSL, CEDPML asserted (write)	54	–	ns
4	CEDPML width asserted	80	–	ns
5	ASL to DSL or CEDPML asserted	44	–	ns
6	ASL, DSL, CEDPML negated to RHWL high	10	–	ns
7	RHWL low to ASL asserted	10	–	ns
8	CEDPML asserted to WRL asserted	1	10	ns
9	WRL negated after ASL, DSL, CEDPML negated	1	10	ns
10	CEDPML asserted to DSACKx asserted	0	–	ns
11	DSACKx negated after ASL, DSL, CEDPML negated	0	60	ns
12	DSL, CEDPML negated to data invalid (data hold)	10	–	ns
13	Data valid after CEDPML asserted	10	–	ns
14	DSL, CEDPML negated to data in high impedance	–	33	ns
15	BUSYL asserted after CEDPML asserted	–	75	ns

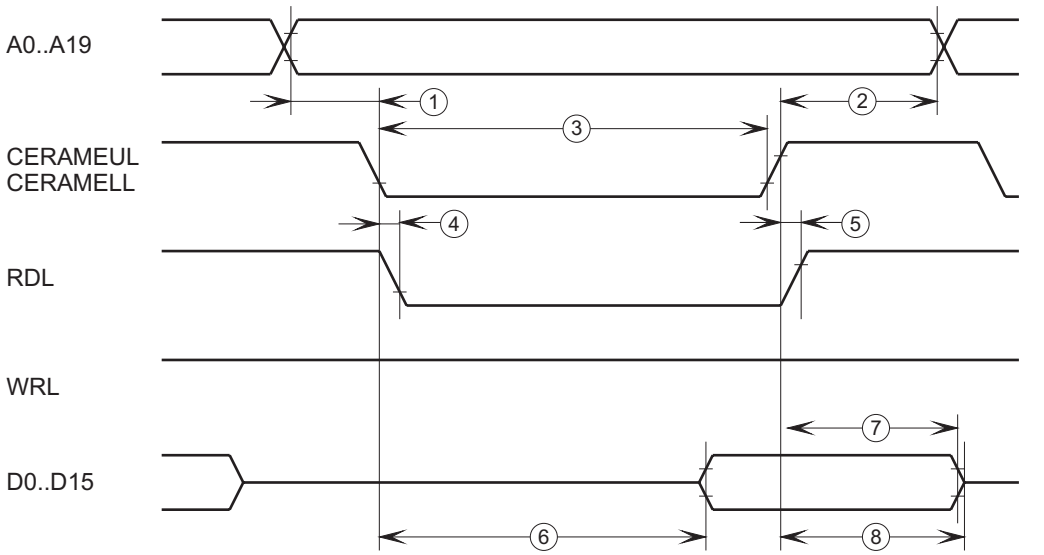


Figure 2-28 RAM extension read access

Table 2-21 RAM extension read access

No.	Characteristic	Min.	Max.	Unit
1	Address valid to CERAMEUL, CERAMELL asserted	10	–	ns
2	CERAMEUL, CERAMELL negated to address invalid (address hold)	10	–	ns
3	CERAMEUL, CERAMELL width asserted	80	–	ns
4	CERAMEUL, CERAMELL asserted to RDL asserted	0	30	ns
5	RDL negated after CERAMEUL, CERAMELL negated	0	30	ns
6	Data valid after CERAMEUL, CERAMELL asserted	–	70	ns
7	CERAMEUL, CERAMELL negated to data invalid (data hold)	0	–	ns
8	CERAMEUL, CERAMELL negated to data in high impedance	–	48	ns

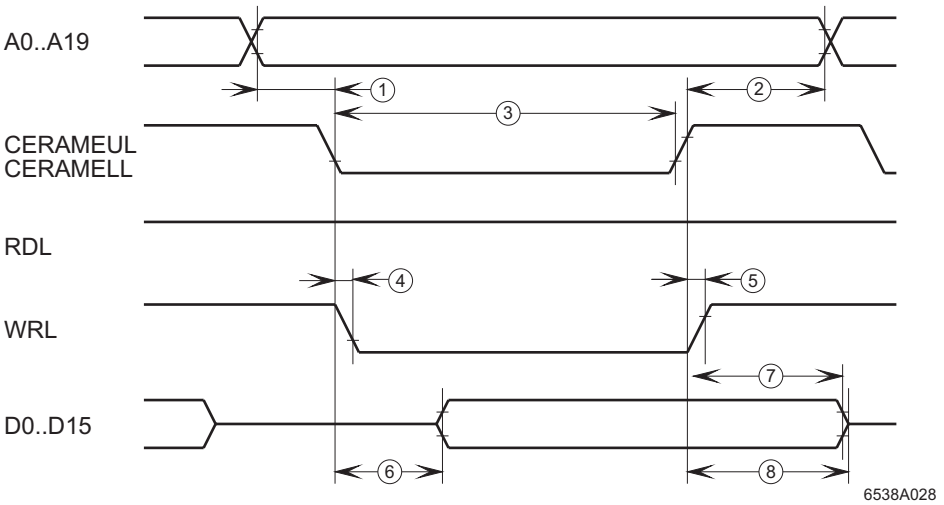


Figure 2-29 RAM extension write access

Table 2-22 RAM extension write access

No.	Characteristic	Min.	Max.	Unit
1	Address valid to CERAMEUL, CERAMELL asserted	10	–	ns
2	CERAMEUL, CERAMELL negated to address invalid (address hold)	10	–	ns
3	CERAMEUL, CERAMELL width asserted	80	–	ns
4	CERAMEUL, CERAMELL asserted to WRL asserted	0	30	ns
5	WRL negated after CERAMEUL, CERAMELL negated	0	30	ns
6	Data valid after CERAMEUL, CERAMELL asserted	–	70	ns
7	CERAMEUL, CERAMELL negated to data invalid (data hold)	10	–	ns
8	CERAMEUL, CERAMELL negated to data in high impedance	–	33	ns

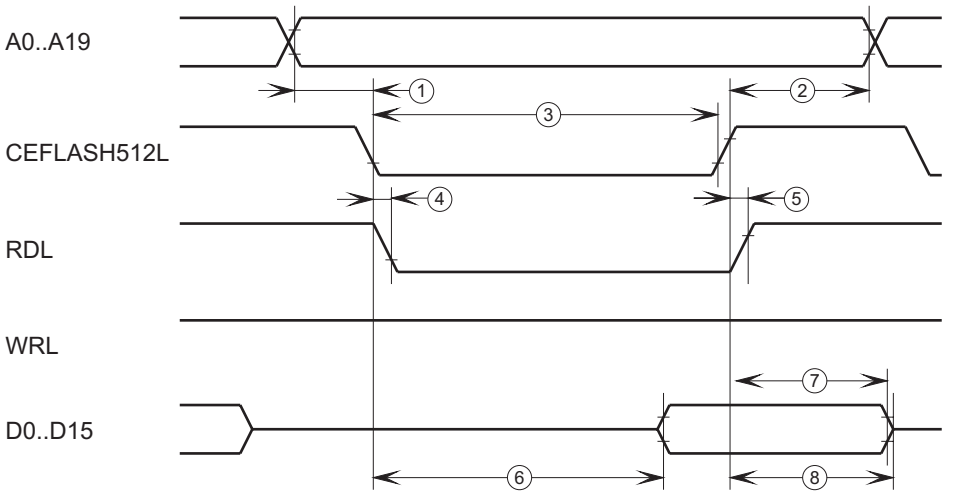


Figure 2-30 16-bit parameter FLASH read access

Table 2-23 16-bit parameter FLASH read access

No.	Characteristic	Min.	Max.	Unit
1	Address valid to CEFLASH512L asserted	–	34	ns
2	CEFLASH512L negated to address invalid (address hold)	–	34	ns
3	CEFLASH512L width asserted	80	–	ns
4	CEFLASH512L asserted to RDL asserted	–	20	ns
5	RDL negated after CEFLASH512L negated	1	10	ns
6	Data valid after CEFLASH512L asserted	–	70	ns
7	CEFLASH512L negated to data invalid (data hold)	0	–	ns
8	CEFLASH512L negated to data in high impedance	–	48	ns

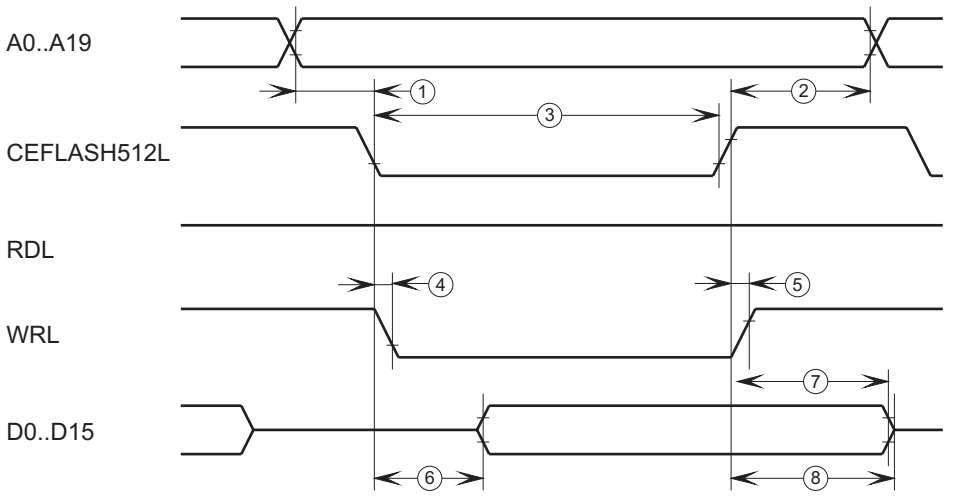


Figure 2-31 16-bit parameter FLASH write access

Table 2-24 16-bit parameter FLASH write access

No.	Characteristic	Min.	Max.	Unit
1	Address valid to CEFLASH512L asserted	–	34	ns
2	CEFLASH512L negated to address invalid (address hold)	–	34	ns
3	CEFLASH512L width asserted	80	–	ns
4	CEFLASH512L asserted to WRL asserted	–	20	ns
5	WRL negated after CEFLASH512L negated	1	10	ns
6	Data valid after CEFLASH512L asserted	22	–	ns
7	CEFLASH512L negated to data invalid (data hold)	10	–	ns
8	CEFLASH512L negated to data in high impedance	–	48	ns

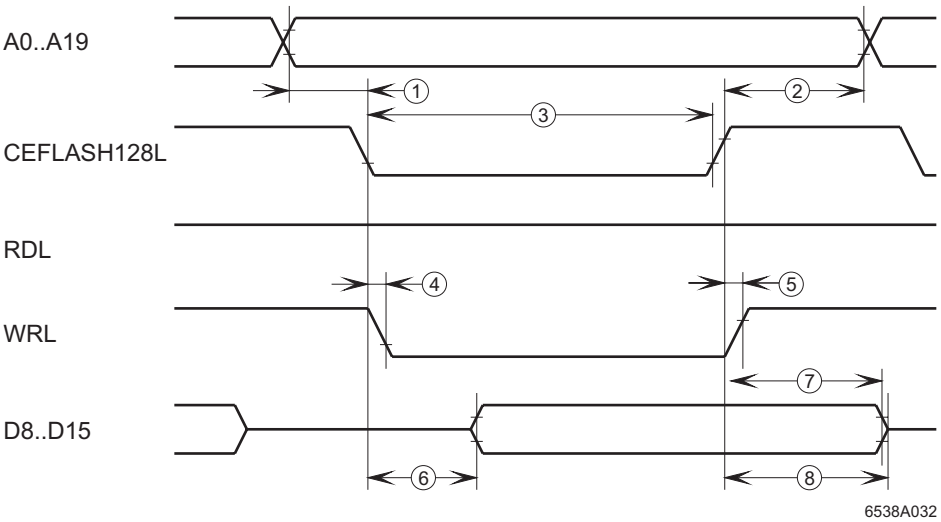


Figure 2-32 IBS SUPI 3 / IBS SRE 1 read access

Table 2-25 IBS SUPI 3 / IBS SRE 1 read access

No.	Characteristic	Min.	Max.	Unit
1	Address valid to CESUPIL, CESREL asserted	10	–	ns
2	CESUPIL, CESREL negated to address invalid (address hold)	10	–	ns
3	CESUPIL, CESREL width asserted	175	–	ns
4	CESUPIL, CESREL asserted to RDL asserted	0	30	ns
5	RDL negated after CESUPIL, CESREL negated	0	30	ns
6	Data valid after CESUPIL, CESREL asserted	–	167	ns
7	CESUPIL, CESREL negated to data invalid (data hold)	0	–	ns
8	CESUPIL, CESREL negated to data in high impedance	–	48	ns

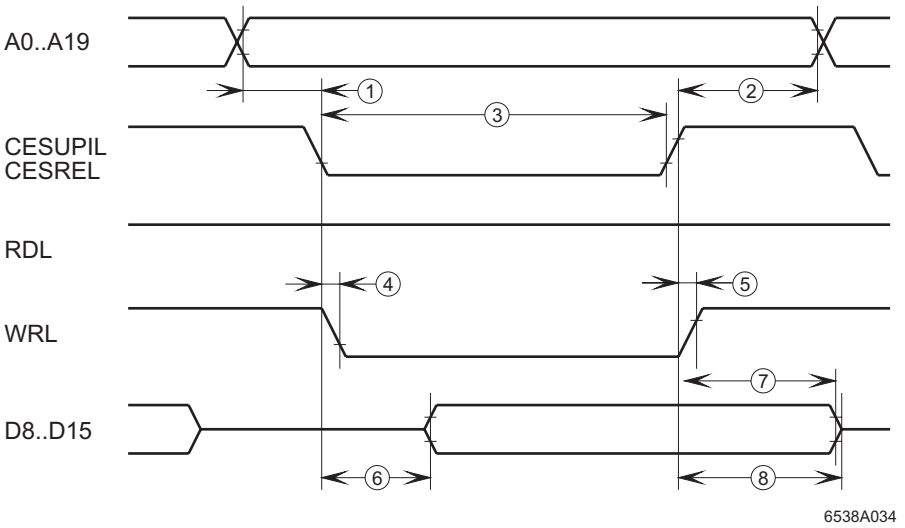


Figure 2-33 IBS SUPI 3 / IBS SRE 1 write access

Table 2-26 IBS SUPI 3 / IBS SRE 1 write access

No.	Characteristic	Min.	Max.	Unit
1	Address valid to CESUPIL, CESREL asserted	10	–	ns
2	CESUPIL, CESREL negated to address invalid (address hold)	10	–	ns
3	CESUPIL, CESREL width asserted	175	–	ns
4	CESUPIL, CESREL asserted to WRL asserted	0	30	ns
5	WRL negated after CESUPIL, CESREL negated	0	30	ns
6	Data valid after CESUPIL, CESREL asserted	–	50	ns
7	CESUPIL, CESREL negated to data invalid (data hold)	10	–	ns
8	CESUPIL, CESREL negated to data in high impedance	–	33	ns

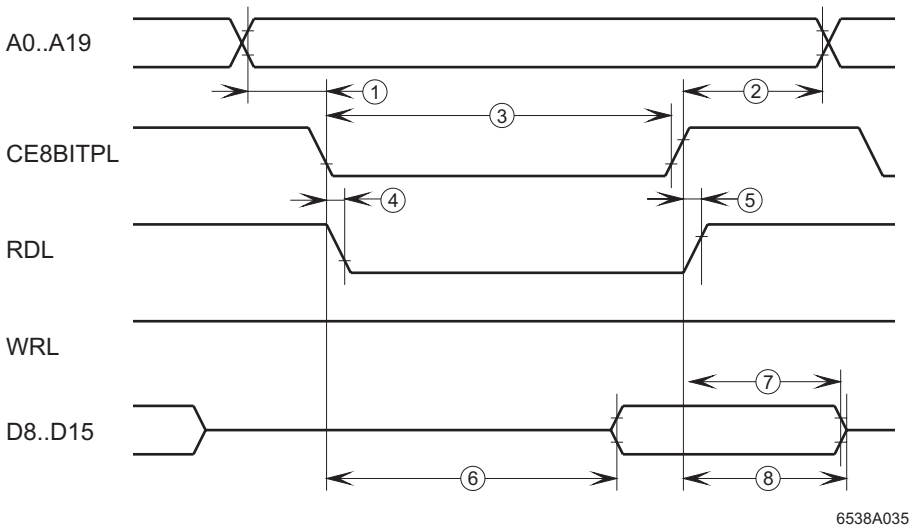


Figure 2-34 8-bit I/O read access

Table 2-27 8-bit I/O read access

No.	Characteristic	Min.	Max.	Unit
1	Address valid to CE8BITPL asserted	10	–	ns
2	CE8BITPL negated to address invalid (address hold)	10	–	ns
3	CE8BITPL width asserted	175	–	ns
4	CE8BITPL asserted to RDL asserted	0	30	ns
5	RDL negated after CE8BITPL negated	0	30	ns
6	Data valid after CE8BITPL asserted	–	167	ns
7	CE8BITPL negated to data invalid (data hold)	0	–	ns
8	CE8BITPL negated to data in high impedance	–	48	ns

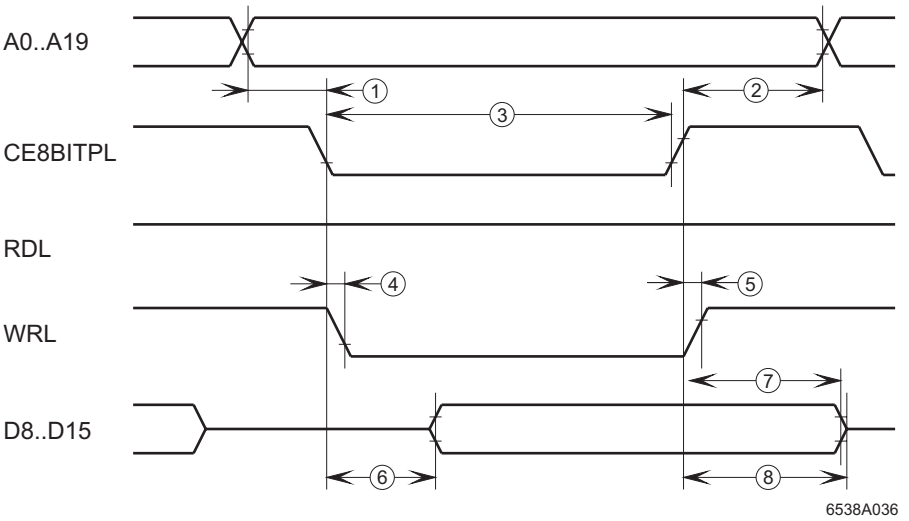


Figure 2-35 8-bit I/O write access

Table 2-28 8-bit I/O write access

No.	Characteristic	Min.	Max.	Unit
1	Address valid to CE8BITPL asserted	10	–	ns
2	CE8BITPL negated to address invalid (address hold)	10	–	ns
3	CE8BITPL width asserted	175	–	ns
4	CE8BITPL asserted to WRL asserted	0	30	ns
5	WRL negated after CE8BITPL negated	0	30	ns
6	Data valid after CE8BITPL asserted	–	50	ns
7	CE8BITPL negated to data invalid (data hold)	10	–	ns
8	CE8BITPL negated to data in high impedance	–	33	ns

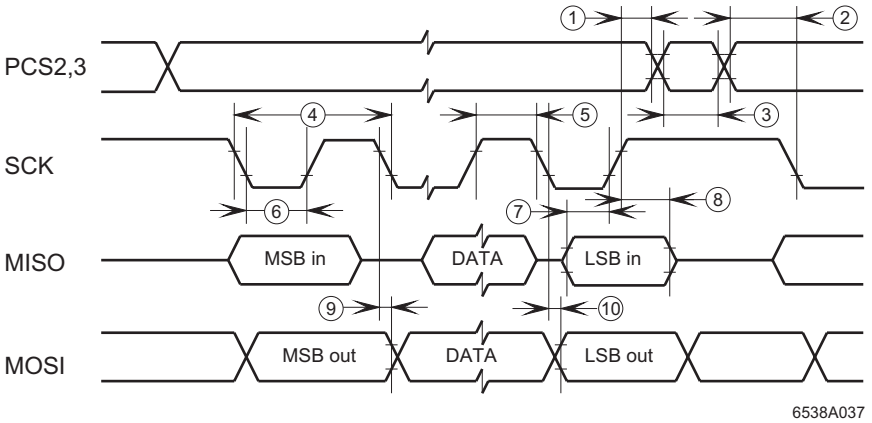


Figure 2-36 SSI serial communication

Table 2-29 SSI serial communication

No.	Characteristic	Min.	Max.	Unit
1	Enable invalid after clock high	–	763	ns
2	Enable valid before clock low	95	–	ns
3	Sequential transfer delay	811	–	ns
4	Cycle time	1526	1907	ns
5	Clock high time	35	–	ns
6	Clock low time	35	–	ns
7	Data in valid to rising edge of SCK (data setup)	30	–	ns
8	Data in invalid after SCK high (data hold)	20	–	ns
9	Data out hold	0	–	ns
10	Data out valid after falling edge of SCK	–	50	ns

2.8 Technical Data

Table 2-30 DC characteristics

Parameter	Min.	Max.	Max.
High-voltage input	0.7 x Vcc	Vcc+0.3	V
Low-voltage input	GND-0.3	0.2 x Vcc	V
Output high voltage			
IOH = -2 mA, Vcc = 4.5 V (DO, CESUPIL, CESREL, clock, CEFLASH512L)	Vcc – 0.8	–	V
IOH = -4 mA, Vcc = 4.5 V (RDL, WRL)	Vcc – 0.8	–	V
IOH = -0.8 mA, Vcc = 4.5 V (all other outputs)	Vcc – 0.8	–	V
Output low voltage			
IOL = 4 mA (RDL, WRL)	–	0.4	V
IOL = 8 mA (CEFLASH512L, CESUPIL, CESREL, SRQMAL, clock)	–	0.4	V
IOL = 1.6 mA (D0..D15, A0..A19, ISPDIN, ISPSCLK, ISPMODE, ISPENL, BD32IFETCH, BD32IPIPE, BD32FREEZE)	–	0.4	V
IOL = 5.3 mA (CERAMELL, CERAMEUL, CE8BITPL, CEDPML, PCS2, PCS3, ASL, DSL, RHWL, SIZEBHWL, TxD, RTS)	–	0.4	V
IOL = 12 mA (MOSI, SCK, DO)	–	0.4	V
Power supply current (Vcc = 5.0 V, CPU clock = 19.923 MHz)	–	180	mA
Input capacitance			
All input pins	–	50	pF
All I/O pins	–	70	pF
Input leakage current			
IRQDPML, IRQHOSTL, IRQSUPIL, SLISRESL,			
SLPDONLYL, ISPDOUT, IRQ1L..IRQ4L, VCCIERRL	-610	2.5	µA
LMODE	-2.5	5000	µA
BUSYL	-5000	2.5	µA
RESETL	-2	2	µA
MISO, RxD, CTS, DI	-2	8.5	µA
DSACK0L, DSACK1L	-7353	2.5	µA

V_{CC} = 5.0 V DC ± 10%, GND = 0 V DC, TA = 0...70°C

Table 2-31 Ambient conditions and system specifications

Temperature – Operation: – Storage:	 0°C to +70°C -25°C to +85°C
Humidity – Operation: – Storage:	 75% 75%
Current consumption	200 mA, typical
Power supply	5 V DC ±10%
Dimensions	50 x 70 mm^2
Interfaces	INTERBUS master interface INTERBUS slave interface (slave extension) Asynchronous serial interface Synchronous serial interface for optical diagnostics (LEDs, LCD) DPM interface
Type of addressing	Physical and logical addressing
Remote bus segments	254, maximum
Number of modules	256 / 512, maximum (basic functions / with extensions)
I/O points	2048 / 4096 / 8192 inputs, maximum (basic functions / with extensions) 2048 / 4096 / 8192 outputs, maximum (basic functions / with extensions)
Diagnostics	Via LEDs, DPM, V.24 and synchronous serial interface
System control	Through message exchange (bit-controlled) via predefined or user-defined command sequences
Supported operating modes	Asynchronous mode with and without consistency locking (polling mode) Asynchronous mode with synchronization pulse (interrupt mode)

3 Structure of the Coupling Memory

The coupling memory is used as the interface between the IBS USC4-2 INTERBUS master board and the host system. The coupling memory is usually implemented on the carrier printed circuit board in the form a a dual-port memory (DPM). Compared to firmware version 4.4 on the IBS USC4-1, firmware version 4.6, which is integrated on the IBS USC4-2, supports twice as many I/O points (8192 inputs and 8192 outputs). This requires the use of an 8-kbyte DPM coupling memory.

Depending on the requirements 2, 4 or 8 kbytes DPM can be addressed by the IBS USC4-2. Using 2 kbytes DPM supports up to 2048 binary inputs and outputs. Using 4 kbytes and 8 kbytes supports 4096 and 8192 binary inputs and outputs, respectively. The dual-port memory is divided into several areas (see Figure 3-2, Figure 3-3 and Figure 3-1). The areas marked "DTA" are used to store process data. The IBS USC4-2 writes the input data supplied by INTERBUS to the "DTA in" area and the host system writes the calculated output data to the "DTA out" area.

Two additional memory areas (marked "SSGI") are used to exchange messages between the IBS USC4-2 and the host system. By means of a handshake method the host system uses these "mailboxes" to request services and receive messages from the IBS USC4-2.

If an INTERBUS slave interface is implemented, the "Slave I/O" area is used to exchange data with the higher-level INTERBUS network. The "Ext. DTA" area can, for example, be used as an additional memory area for user-defined functions. These are integrated in the INTERBUS Generation 4 firmware and in the IBS CMD G4 E user interface.

The communication protocols between the IBS USC4-2 and the host system, as well as the provision of status information is handled by means of access to the "Register" area. The registers are explained on the following pages.

The supported DPM chips are listed in Table 2-6 on page 2-12,

Write access to the "reserved" or "res." memory areas, registers or bits are not permitted.

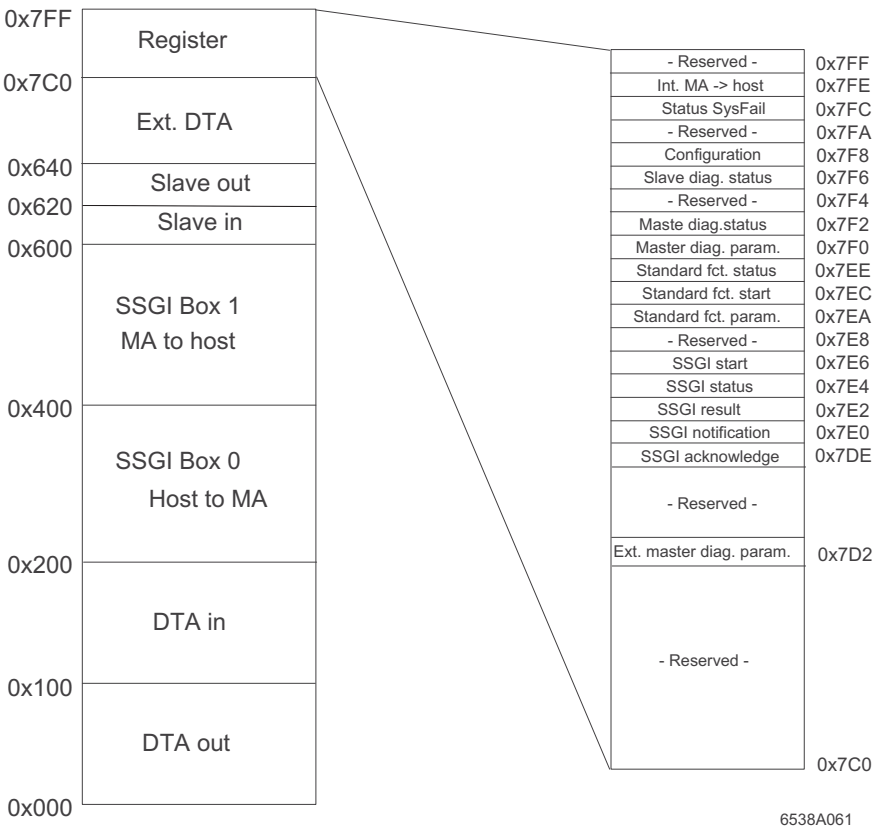


Figure 3-1 Memory segmentation for 2 kbytes DPM

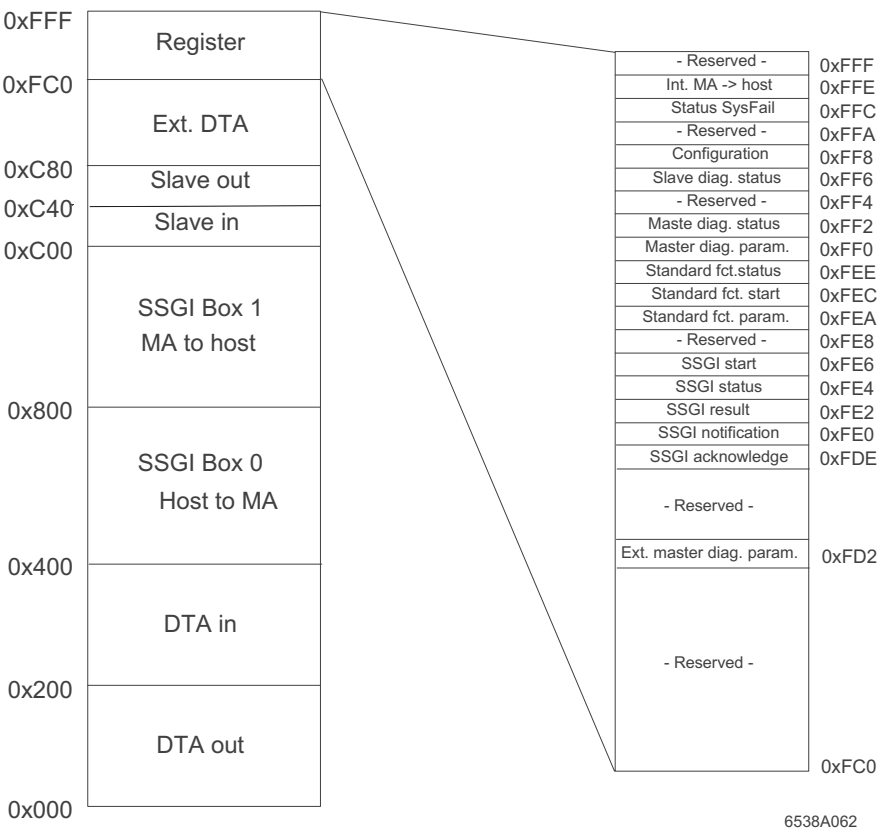


Figure 3-2 Memory segmentation for 4 kbytes DPM

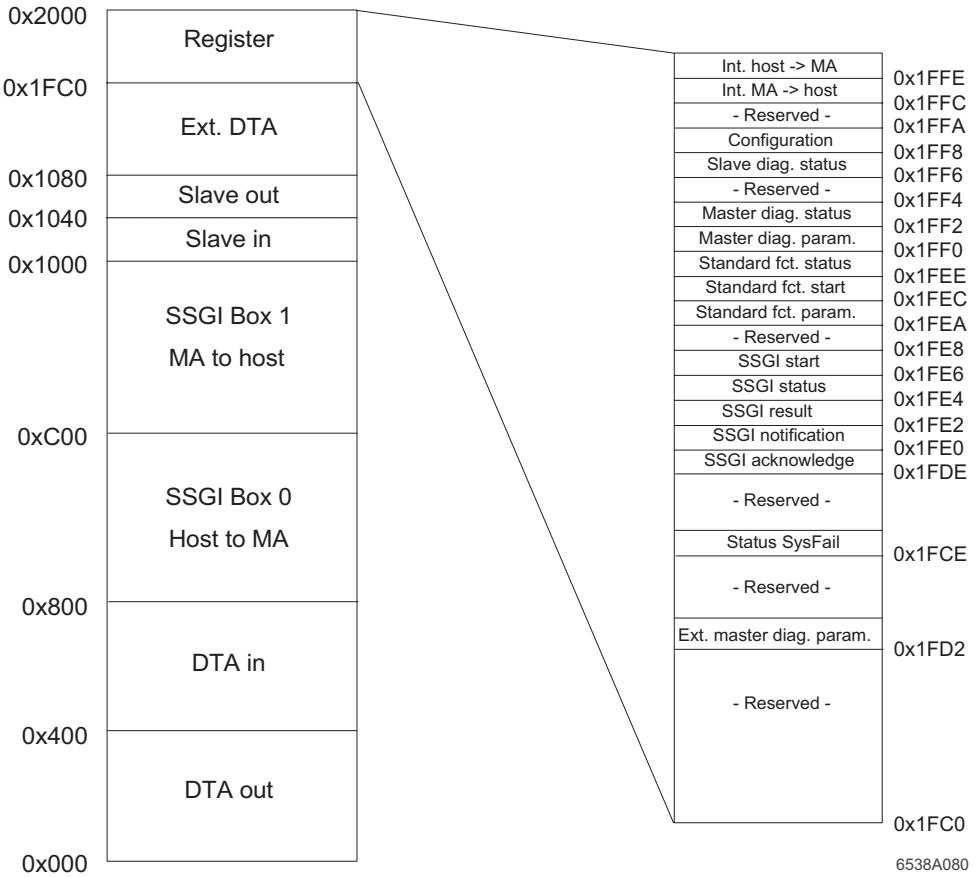


Figure 3-3 Memory segmentation for 8 kbytes DPM

3.1 Register Description

3.1.1 Interrupt Register Host → Master (INT_H_MA)

This register and the INT_MA_H register are used to generate interrupt registers for **asynchronous mode with synchronization** (see also Section 4.5, "Asynchronous Data Exchange With Sychronization Pulse").

Address 2 kbytes DPM: $7FF_{hex}$
Address 4 kbytes DPM: FFF_{hex}
Address 8 kbytes DPM: $1FFF_{hex}$

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x

The register may contain the following:

APPLICATION_READY_COMMAMD 20_{hex}

3.1.2 Interrupt Register Master → Host (INT_MA_H)

This register is used during the start-up phase to synchronize the host system and the IBS USC4-2. After a power-up reset and a successfully completed selftest, the IBS USC4-2 writes the value $C3_{hex}$ to this register.

Address 2 kbytes DPM: $7FE_{hex}$
Address 4 kbytes DPM: FFE_{hex}
Address 8 kbytes DPM: $1FFE_{hex}$

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x

The register may contain the following:

MASTER_READY_COMMAND $C3_{hex}$
DATA_CYCLE_READY_COMMAMD 10_{hex}

3.1.3 Status SysFail Register

This register indicates any malfunctions in the host system.

Address 2 kbytes DPM: $7FC_{hex}$

Address 4 kbytes DPM: FFC_{hex}

Address 8 kbytes DPM: $1FFC_{hex}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res.	res.	res.	x	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.

Bit 12 = 1 Malfunction in the host system

= 0 No malfunction in the host system

The IBS USC4-2 sets this bit if a malfunction in the host system is reported by the IRQHOSTL interrupt. In this case, all INTERBUS device outputs are set to "0". Additionally, the "HF" diagnostic LED lights up.

3.1.4 Configuration Register

This register indicates whether the IBS USC4-2 has completed either a stored parameterization process or one executed by the IBS SWT CMD G4 E user interface.

Address 2 kbytes DPM: $7F8_{hex}$

Address 4 kbytes DPM: $FF8_{hex}$

Address 8 kbytes DPM: $1FF8_{hex}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	x	res.

Bit 1 **DPM node par ready 1**

= 1 IBS USC4-2 parameterized

= 0 IBS USC4-2 not parameterized

If a parameterization has been stored in the IBS USC4-2 parameterization memory, the IBS USC4-2 begins to process the commands stored in the parameterization memory immediately after reaching the READY state. The IBS USC4-2 sets bit 1 once all commands in the parameterization memory have been processed.

3.1.5 Slave Diagnostic Status Register

This register contains information on the status of the optional slave interface in relation to a higher-level INTERBUS network. The content of this register is maintained by the IBS USC4-2.

Address 2 kbytes DPM: $7F6_{hex}$

Address 4 kbytes DPM: $FF6_{hex}$

Address 8 kbytes DPM: $1FF6_{hex}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	x	x	x	x	x

Bit 0 **COPY**

= 1 Data is exchanged between the IBS USC4-2 and the slave interface. The higher-level INTERBUS network is operating.

= 0 No data is exchanged between the IBS USC4-2 and the slave interface. The higher-level INTERBUS network is not operating.

Bit 1 **FAIL**

= 1 The higher-level INTERBUS network has been stopped due to a bus error or alarm stop. Data is no longer exchanged between the IBS USC4-2 and the slave interface. The output data of the slave interface has been set to "0".

= 0 No error in the higher-level INTERBUS network.

Bit 2 **READY TO COPY**

= 1 The slave interface has been parameterized successfully.

= 0 The slave interface has not yet been parameterized.

Bit 3 **POWER ON**

= 1 The power supply for the slave interface is on.

= 0 The power supply for the slave interface is off.

Bit 4 **READY**

The content of the slave diagnostic status register has been initialized.

The content of the slave diagnostic status register has not yet been initialized.

3.1.6 Master Diagnostic Status Register

This register contains information on the status of the IBS USC4-2 master board. The meaning of the bits is shown in the set state ("1"). The content of this register is maintained by the IBS USC4-2. In the event of an error additional information is available in the master diagnostic parameter register and in the extended master diagnostic parameter register.

Address 2 kbytes DPM: $7F2_{hex}$

Address 4 kbytes DPM: $FF2_{hex}$

Address 8 kbytes DPM: $1FF2_{hex}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res.	x	x	res.	res.	x	x	x	x	x	x	x	x	x	x	x

Bit 0	(USER)	User error/parameterization error
Bit 1	(PF)	Peripheral fault
Bit 2	(BUS)	Bus error
Bit 3	(CTRL)	Error on the IBS USC4-2
Bit 4	(DETECT)	Diagnostic routine active
Bit 5	(RUN)	Data transmission active
Bit 6	(ACTIVE)	Selected INTERBUS configuration ready to operate
Bit 7	(READY)	IBS USC4-2 ready to operate
Bit 8	(BSA)	Bus segment(s) aborted
Bit 9	(BASP/SYSFAIL)	Malfunction in the host system detected; outputs reset on INTERBUS
Bit 10	(RESULT)	Negative result of a standard function
Bit 13	(WARNING)	Specified bus waiting time exceeded
Bit 14	(QUALITY)	Specified error density exceeded This bit is set if more than 20 errors occur in one million INTERBUS cycles.

3.1.7 Master Diagnostic Parameter Register

Address 2 kbytes DPM: $7F0_{hex}$
Address 4 kbytes DPM: $FF0_{hex}$
Address 8 kbytes DPM: $1FF0_{hex}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Depending on the type of error, the error code or error location is indicated in this register. The content of this register is maintained by the IBS USC4-2. For some types of error additional information is available in the extended master diagnostic parameter register.

3.1.8 Standard Function Status Register

The IBS USC4-2 uses bits 0..6 of this register to indicated and monitor processing of the standard functions activated in the standard function start register. Bit 15 is used to handle a protocol (see Section 4) for the exchange of process data between the IBS USC4-2 and the host system.

Address 2 kbytes DPM: $7EE_{hex}$
Address 4 kbytes DPM: FEE_{hex}
Address 8 kbytes DPM: $1FEE_{hex}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	res.	res.	res.	res.	res.	res.	res.	res.	x	x	x	x	x	x	x

Bit 0	Start_Data_Transfer_Request status bit
Bit 1	Alarm_Stop_Request, Activate_Configuration_Request status bit
Bit 2	Confirm_Diagnostics_Request status bit
Bit 3	Control_Active_Configuration_Req Off status bit
Bit 4	Control_Active_Configuration_Req On status bit
Bit 5	Control_Active_Configuration_Req Disable status bit
Bit 6	Control_Active_Configuration_Req Enable status bit
Bit 15	Cons state bit for consistency locking

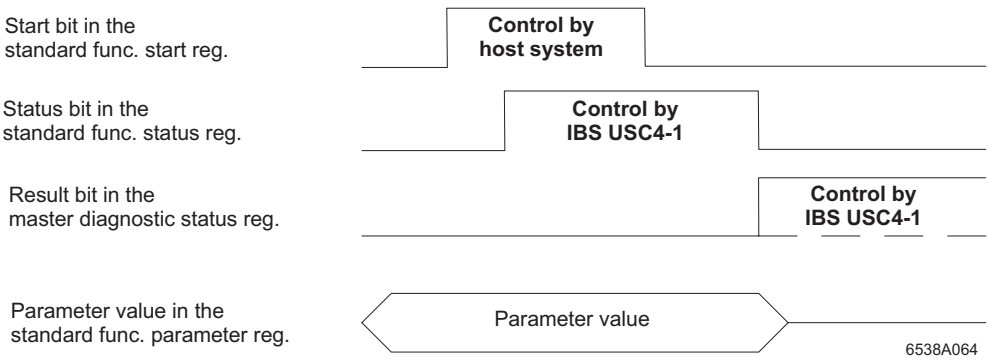


Figure 3-4 Execution of a standard function with parameter transfer

Figure 3-4 illustrates the handshake mechanism when using standard functions. "0" in bit 10 (RESULT) of the master diagnostic status register indicates that the standard function was completed successfully.

3.1.9 Standard Function Start Register

Using this register and the standard function parameter register, the IBS USC4-2 can be controlled without using the SSGI "mailboxes". Various frequently used commands or command sequences can be executed using these two registers. This reduces the demands for requesting services, especially for bit-oriented host systems. Another start register with additional parameter and result registers for controlling up to 16 standard functions can be defined using the IBS CMD G4 E user interface.

For additional information on standard functions, please refer to the IBS CMD G4 E reference manual (Order Designation IBS CMD SWT G4 UM E, Order No. 27 22 25 0).

Address 2 kbytes DPM: $7EC_{hex}$
Address 4 kbytes DPM: FEC_{hex}
Address 8 kbytes DPM: $1FEC_{hex}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	res.	res.	res.	res.	res.	res.	res.	res.	x	x	x	x	x	x	x

Bit 0 **Start_Data_Transfer_Req** start bit

Starts data transmission. Prerequisite: IBS USC4-2 is in the ACTIVE state.

Parameters: None

Bit 1 **Alarm_Stop_Req**, **Activate_Configuration_Req** start bit

Stops data transmission; sets the outputs of all INTERBUS devices to "0" and activates a new configuration frame. The module then is in the ACTIVE state.

Parameters: Number of the configuration frame to be loaded (e.g., "1")

Bit 2 **Confirm_Diagnostics_Req** start bit

This bit updates the content of the diagnostic registers and the diagnostic displays.

Parameters: None

Bit 3 **Control_Active_Configuration_Req Off** start bit

This bit can be used to switch off INTERBUS segments.

Parameters: The segment number should be stored in the high-order byte and the position in the low-order byte.

When a local bus device is switched off, all the devices in the relevant local bus are switched off.

If a remote bus device or a bus coupler is added, both the affected device and the outgoing INTERBUS interface and therefore all subsequent INTERBUS devices are switched off.

Bit 4 **Control_Active_Configuration_Req On** start bit

This bit can be used to switch on the INTERBUS segments that have been switched off.

Parameters: See bit 3

Bit 5 **Control_Active_Configuration_Req Disable** start bit

The device specified as the parameter is disabled in the configuration frame. It must not remain physically in the data ring and must be jumpered manually.

Parameters: The segment number should be stored in the high-order byte and the position in the low-order byte.

Bit 6 **Control_Active_Configuration_Req Enable** start bit

The device specified as the parameter is enabled again in the configuration frame. It must be inserted again manually in the data ring.

Parameters: See bit 5

Bit 15 **Cons activate bit** for consistency locking

Bit 15 is used to handle a protocol (see Section 4) for the exchange of process data between the IBS USC4-2 and the host system.

3.1.10 Standard Function Parameter Register

Address 2 kbytes DPM: $7EA_{hex}$
Address 4 kbytes DPM: FEA_{hex}
Address 8 kbytes DPM: $1FEA_{hex}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Used by the host system to transfer parameters for the standard functions activated using the standard function start register.

3.1.11 SSGI Start Register

The following three registers are used for handshaking when exchanging messages between the host system and the IBS USC4-2 over the SSGI.

Address 2 kbytes DPM: $7E6_{hex}$
Address 4 kbytes DPM: $FE6_{hex}$
Address 8 kbytes DPM: $1FE6_{hex}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res.	res.	res.	res.	res.	res.	res.	x	res.	res.	res.	res.	res.	res.	res.	x

Bit 0 Start bit for the **test mode** action
The connected INTERBUS is automatically started.

Bit 8 Start bit for box 0 of the SSGI (see Section 4.1.1 on page 4-2)

3.1.12 SSGI Status Register

Address 2 kbytes DPM: $7E4_{hex}$
Address 4 kbytes DPM: $FE4_{hex}$
Address 8 kbytes DPM: $1FE4_{hex}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res.	res.	res.	res.	res.	res.	res.	x	res.	res.	res.	res.	res.	res.	res.	x

Bit 0 Status bit for the **test mode** action
= 1 Automatic startup currently being executed
= 0 Automatic startup currently not being executed
Bit 8 Status bit for box 0 of the SSGI (see Section 4.1.1 on page 4-2)

3.1.13 SSGI Result Register

Address 2 kbytes DPM: $7E2_{hex}$
Address 4 kbytes DPM: $FE2_{hex}$
Address 8 kbytes DPM: $1FE2_{hex}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res.	res.	res.	res.	res.	res.	res.	x	res.	res.	res.	res.	res.	res.	res.	x

Bit 0 Result bit for the **test mode** action
= 1 Error during automatic configuration
= 0 Automatic configuration completed successfully
Bit 8 Result bit for box 0 of the SSGI (see Section 4.1.1 on page 4-2)

3.1.14 SSGI Notification Register

Address 2 kbytes DPM: $7E0_{hex}$
Address 4 kbytes DPM: $FE0_{hex}$
Address 8 kbytes DPM: $1FE0_{hex}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res.	res.	res.	res.	res.	res.	res.	x	res.	res.	res.	res.	res.	res.	res.	res.

Bit 8 Notify bit for box 1 of the SSGI (see Section 4.1.2 on page 4-3)

3.1.15 SSGI Acknowledge Register

Address 2 kbytes DPM: $7DE_{hex}$
Address 4 kbytes DPM: FDE_{hex}
Address 8 kbytes DPM: $1FDE_{hex}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res.	res.	res.	res.	res.	res.	res.	x	res.	res.	res.	res.	res.	res.	res.	res.

Bit 8 Acknowledge bit for box 1 of the SSGI (see Section 4.2.2 on page 4-7)

3.1.16 Extended Master Diagnostic Parameter Register

Address 2 kbytes DPM: $7D2_{hex}$
Address 4 kbytes DPM: $FD2_{hex}$
Address 8 kbytes DPM: $1FD2_{hex}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Depending on the type of error this register provides additional information on the error indicated in the master diagnostic status register and master diagnostic parameter register. It is used for future extended diagnostic functions of INTERBUS slaves.

For the exact meaning of the diagnostic data contained in this register, please refer to the data sheet or user manual of the relevant INTERBUS slave.

4 Communication Between the Host System and the IBS USC4-2

When using a DPM, data is exchanged between the host system and the IBS USC4-2 via two interfaces:

– **S**tandard **Sig**nal **I**nterface (SSGI) for exchanging messages (e.g., service requests on the master board)
– **Data** Interface (DTA) for exchanging process data

Each interface has its own memory area in the DPM, which is divided into a transmit and receive area.

The IBS USC4-2 stores the input data provided by INTERBUS in the "DTA in" area. The host system writes the calculated output data to the "DTA out" area.

Box 0 of the SSGI is used for message transfer from the host system to the IBS USC4-2. Box 1 transfers messages from the IBS USC4-2 to the host system. A handshake protocol, which is described on the following pages, is used for this purpose.

The base addresses and the size of the individual memory areas depend on the size of the implemented coupling memory (see Figure 3-1 on page 3-2 to Figure 3-3 on page 3-4).

4.1 Message Exchange Over the SSGI

4.1.1 Transmitting Messages to the IBS USC4-2

The host application must first check whether the corresponding box (SSGI box 0 host to MA) is free. This box is free if the SSGI start bit and the SSGI status bit both have content "0". After that the host system can enter a message (service request) in box 0 and set the SSGI start bit.

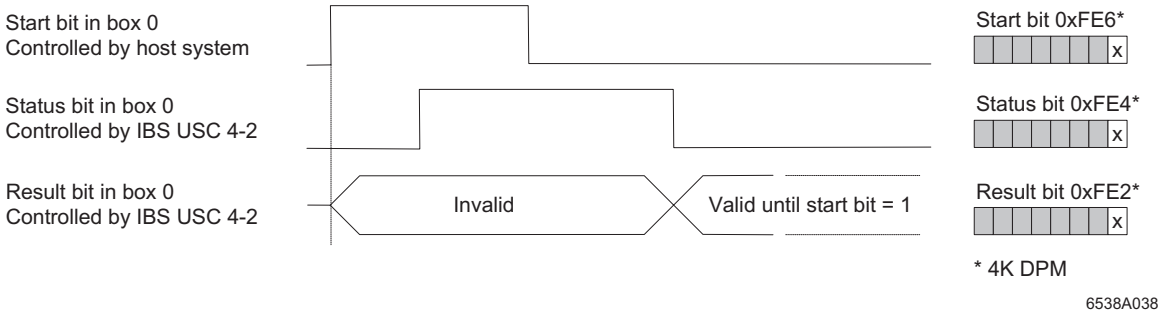


Figure 4-1 The host system transmits a message

By setting the SSGI status bit the IBS USC4-2 indicates that is has detected and is processing the service request. The host system must now clear the SSGI start bit to indicate to the IBS USC4-2 that is has detected service request processing.

Once the SSGI status bit has been cleared by the IBS USC4-2, the SSGI result bit becomes valid. If this bit equals "0" during the period of validity, the message has been read completely by the IBS USC4-2 and box 0 is free again. If the SSGI result bit equals "1" during the period of validity, an error occurred (see Figure 4-1).

4.1.2 Receiving Messages From the IBS USC4-2

The IBS USC4-2 sets the SSGI notify bit to inform the host system that there is a message in SSGI box 1. The host system then sets the SSGI acknowledge bit to inform the IBS USC4-2 that is has detected the message.

Once the IBS USC4-2 has detected that the SSGI acknowledge bit is set, it resets the SSGI notify bit. Once the host system has processed the message or/and once SSGI box 0 is free again, the host can reset its SSGI acknowledge bit (see Figure 4-2).

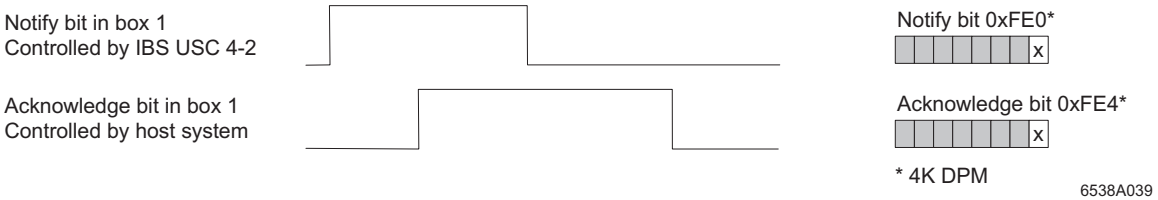


Figure 4-2 The host system receives a message

If, in the event of a large number of messages arriving quickly one after the other, the host system processing speed is significantly slower than that of the IBS USC4-2, box 1 may not yet have been enabled when a message arrives (SSGI acknowledge bit = "1"). In this case, the IBS USC4-2 buffers the new message and transmits it to the host system at a later point in time. However, the buffer is limited in size.

4.2 Exchanging Process Data Over the Data Interface

Process data is updated by the IBS USC4-2 synchronously with the INTERBUS data cycles, but asynchronously with the host system's random access to the process image. An optional signal protocol can be used to lock access to the coupling memory (DPM) and thus enable the host system to access the complete consistent process image (see Section 4.4 on page 4-11).

There are two different methods of storing process data in the coupling memory. Figure 4-3 shows the structure of the DPM memory allocation with physical addressing (standard settings) of the process data. The firmware also supports user-defined logical addressing. The user can freely determine the storage address of the process data within the relevant DPM area. This is especially easy using the CMD software tool (IBS CMD SWT G4 E, Order No. 27 21 44 2).

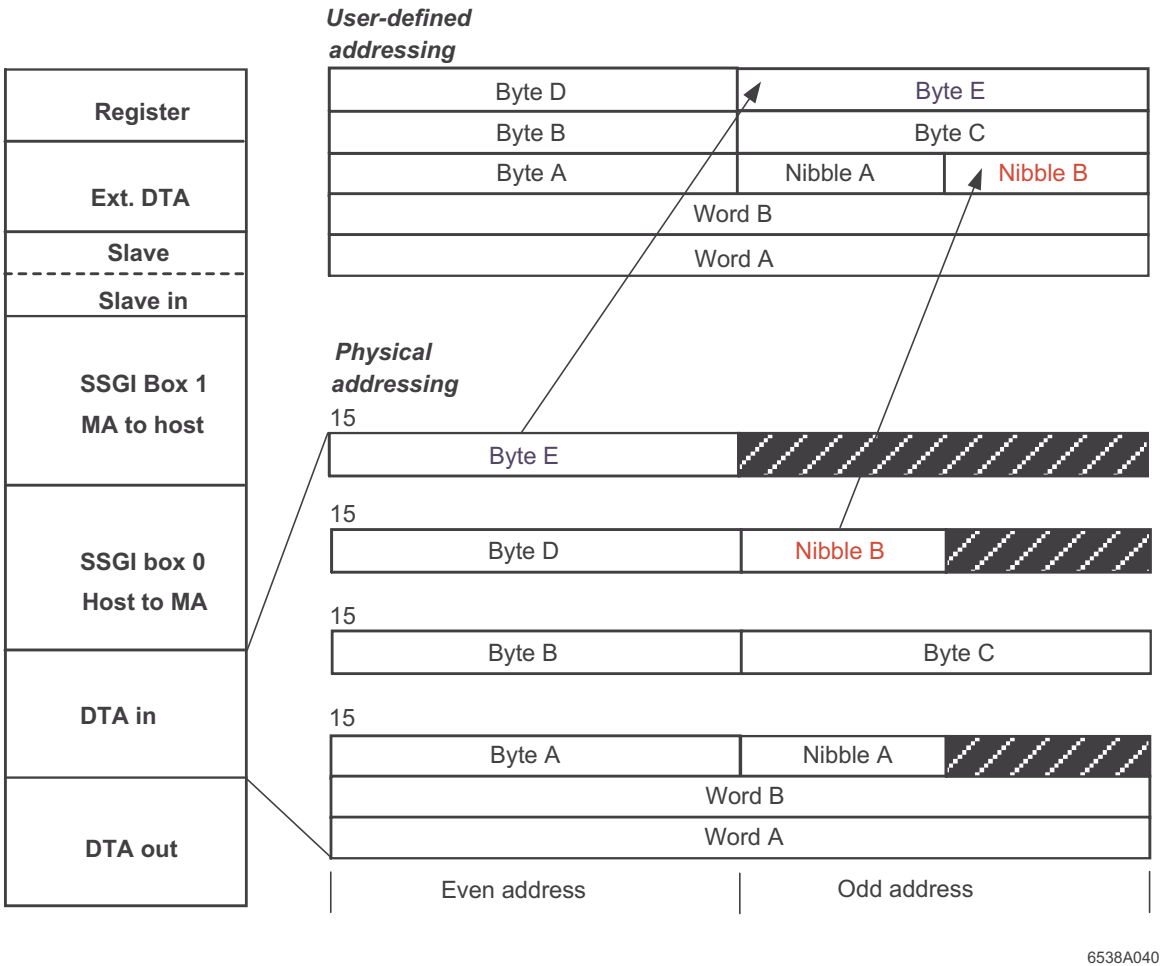


Figure 4-3 Different methods of addressing process data in the coupling memory

4.2.1 Reading and Writing System Variables

The Set_Value_Req (0750_{hex}) and Read_Value_Req (0351_{hex}) services are used to read and write system variables (see IBS SYS FW G4 UM E).

Table 4-1 System variables for INTERBUS operation

Var. ID [hex]	System Variable	Value Range
2200_{hex}	Operating mode 16-bit value Activation and deactivation of the synchronization interrupt (see Section 4.5 on page 4-15)	0000_{hex}: OFF 0600_{hex}: ON
2210	Default cycle time (update time T_{UP}) 32-bit value [µs] The cycle time is the actual time between the start of two successive INTERBUS data cycles (see Section 4.2.2).	0000 0000_{hex} to 0001 $FBD0_{hex}$ (corresponds to 0 µs to 130 ms) Default: automatically when bus is created
2211	Bus timeout (T_{TO_BUS}) 32-bit value [µs] If no error-free INTERBUS data cycle can be executed within this time, the IBS USC4-2 stops transmission and triggers an INTERBUS reset (see Section 4.2.2).	0000 0000_{hex} to FFFF $FFFF_{hex}$ (corresponds to 0 µs to 71 min) Default: 200 ms
2212	Bus warning time (T_{WA_BUS}) 32-bit value [µs] If no error-free INTERBUS data cycle can be executed within this time, the IBS USC4-2 sets the warning bit in the diagnostic status register (see Section 4.2.2).	0000 0000_{hex} to FFFF $FFFF_{hex}$ (corresponds to 0 µs to 71 min) Default: 0 (deactivated)
2215	Error message $0BD2_{hex}$ activated/deactivated Displayed if not INTERBUS data cycle was transmitted within the bus warning time (variable ID 2212_{hex})	0000 0001_{hex}: Message activated 0000 0000_{hex}: Message deactivated
2216	Actual cycle time 32-bit value [µs] If the specified cycle time (variable ID 2210_{hex}) cannot be maintained, the actual time between the start of two successive INTERBUS data cycles is shown here.	Read only

4.2.2 Timing and Monitoring Mechanisms

The IBS USC4-2 firmware has various timing and monitoring mechanisms for the implementation of user-defined time behavior.

The following monitoring times represent layer 2 operating parameters and can be defined by the user as system variables using the Set_Value service.

Default Cycle Time (Update Time T_{UP})

The default cycle time is the time that should elapse between the start of two successive bus cycles. It must be longer than the duration of the INTERBUS data cycle and is set by the IBS USC4-2 to a value determined by the connected INTERBUS configuration. This value can be read using the Read_Value service (0351_{hex}).

The default cycle time can be parameterized using the Set_Value service.

Parameter value:	32 bits
Settable values:	T_{UP} * 1 µs
Standard value:	Determined by the system using the configuration

Bus Warning Time (T_{WA_BUS})

The bus warning time is the the maximum time that may elapse between two valid INTERBUS data cycles before the warning bit (bit 13) in the master diagnostic status register indicates to the user that the transmission quality has deteriorated.

Exceeding this time does not lead to a fatal bus error. The standard settings made by the IBS USC4-2 for this system variable is 0, i.e., this monitoring mechanism is switched off.

The bus warning time can be parameterized using the Set_Value service. It is a preliminary stage for the bus timeout.

Parameter value:	32 bits
Settable values:	T_{WA_BUS} * 1 µs
Standard value:	0 (no monitoring)

Bus Timeout (T_{TO_BUS})

The bus timeout is the maximum time that may elapse between two valid INTERBUS data cycles.

Exceeding this time leads to a fatal bus error (e.g., too much EMI, cable break, power supply failure etc.). This error is reported by the BUS bit (bit 2) in the master diagnostic status register.

The bus timeout can be parameterized using the Set_Value service. As a basic setting, the IBS USC4-2 sets the bus timeout to a value that is twenty times the standard value.

Parameter value:	32 bits
Settable values:	T_{TO_BUS} * 1 µs
Standard value:	200 ms

The following diagram illustrates the meaning of the individual monitoring times.

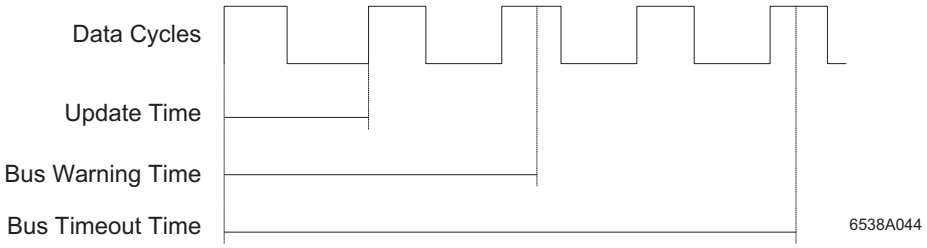


Figure 4-4 Monitoring times

Application Timeout

In "asynchronous mode with synchronization pulse" the INTERBUS system is stopped with a sychronization error (error code: $0BDE_{hex}$) after the application timeout (0.5 * bus timeout) has elapsed, if the host system does not trigger an interrupt (APPLICATION_READY_COMMAMD; see Section 3) in the direction of the INTERBUS master within this time. In this way the IBS USC4-2 monitors the maximum time that may elapse between the interrupt of the master and the interrupt of the host system.

4.2.3 Parallel and Sequential Transmission of Process Data

These terms indicate the moment at which process data is copied to or from the DPM.

In parallel transmission, process data is read from the DPM (OUT data) and written to the DPM (IN data) after an INTERBUS data cycle has started.

In sequential transmission, process data is written to the DPM (IN data) after an INTERBUS data cycle has been completed or read from the DPM (OUT data; Figure 4-5) before an INTERBUS data cycle has been started.

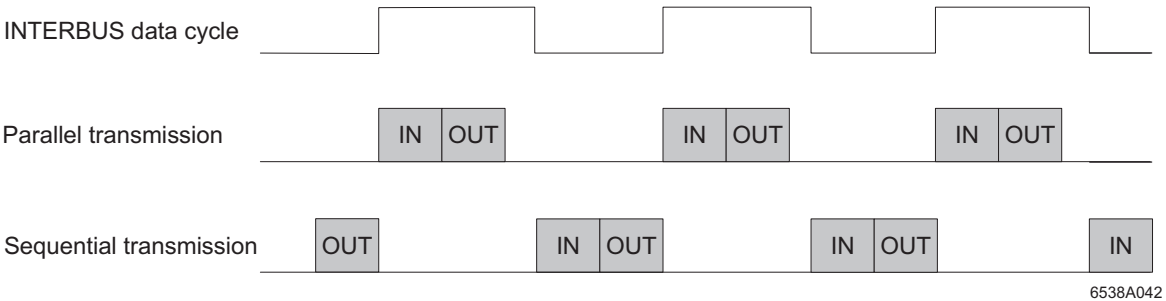


Figure 4-5 Transmission of process data between the IBS USC4-2 and the DPM

The type of transmission (parallel or sequential) can be set for each process data item. This means that parallel and sequential transmission can be combined in the entire system.

By default, all process data is transmitted in parallel. During user-defined addressing, sequential transmission can be selected using the process data description. For this purpose, bit 6 is set in the "bit position" parameter of the individual process data references (see description of the "Load_Process_Data_Reference_List_Req" service, 0325_{hex}). This can also easily be done when setting the parameters using the IBS CMD G4 E user interface.

Using the sequential transmission method increases the cycle time, as additional time is required to copy the data before and after an INTERBUS data cycle.

The following diagram (Figure 4-6) directly compares parallel and sequential transmission and illustrates the number of INTERBUS data cycles that is required to transport process data from the DPM to an INTERBUS device and vice versa.

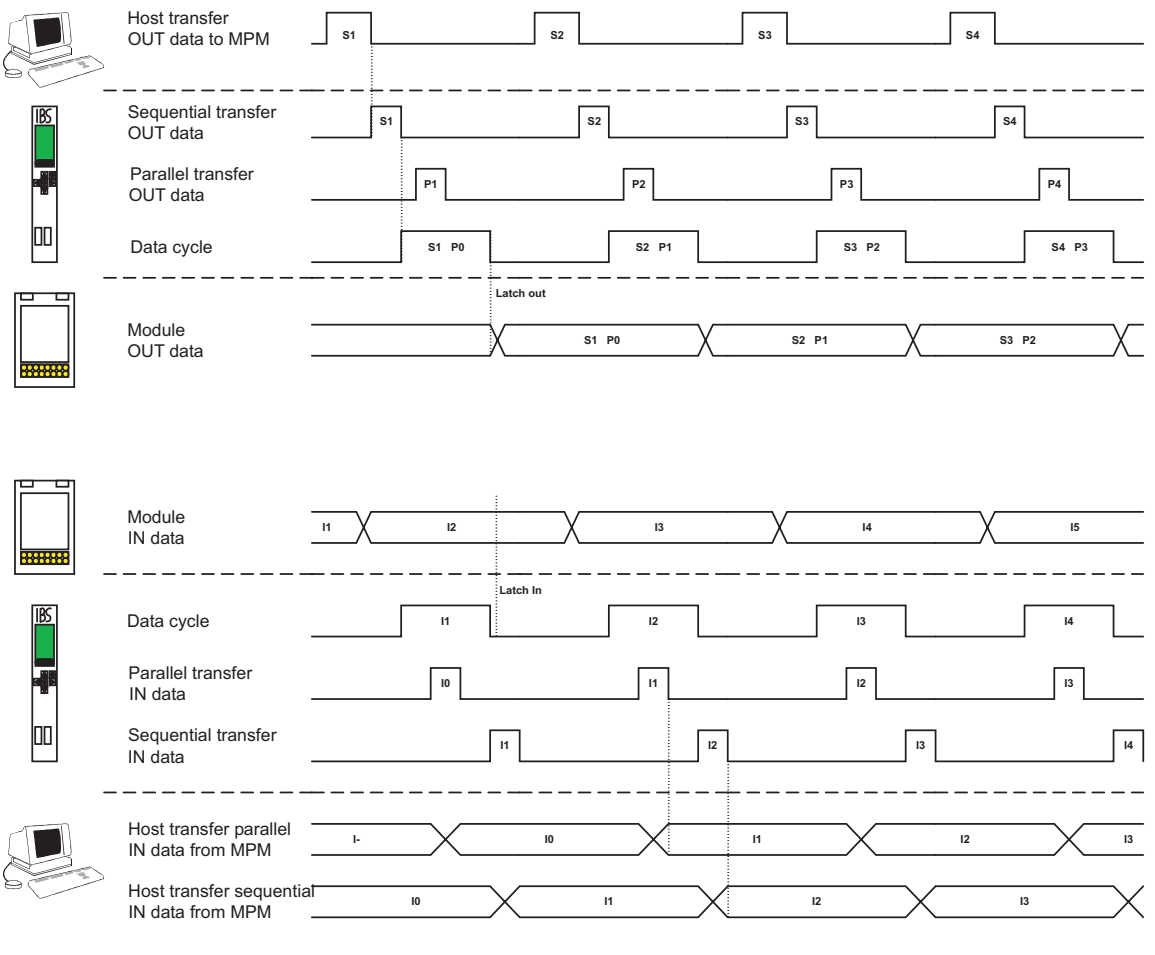


Figure 4-6 Transmission of process data between the host system and INTERBUS devices

Please note that process data must be written to the DPM by the host system before starting the transmission mechanism and must not be read from the DPM until transmission is completed.

Possible module filter times have not been taken into account in Figure 4-6.

4.3 Asynchronous Data Exchange Without Consistency Locking

In "asynchronous" mode, process data is updated by the IBS USC4-2 synchronously with the INTERBUS data cycles, but asynchronously with the host system's random access to the process image. Data consistency is 8 bits in this mode.

4.4 Asynchronous Data Exchange With Consistency Locking

The **optional** signal protocol described in the following allows for locking access to the coupling memory in such a way that the host system can access a process image that is consistent in terms of time.

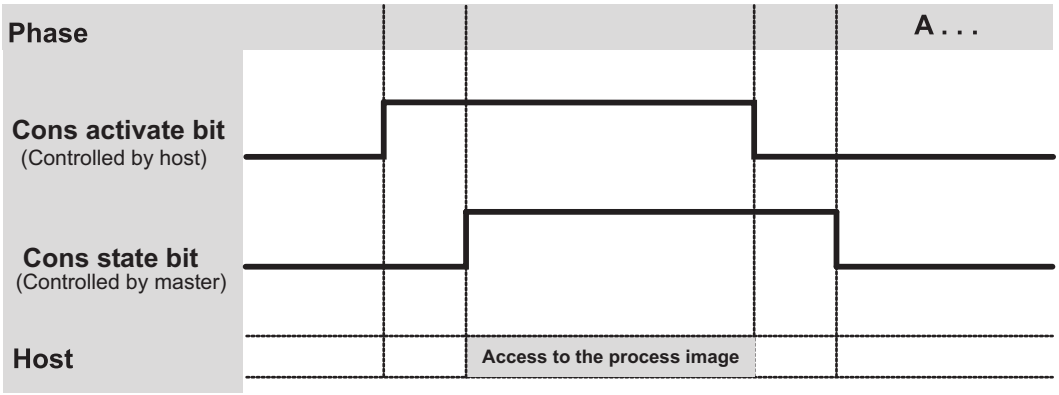


Figure 4-7 Access to the process image in "asynchronous mode with consistency locking"

The cons activate bit is bit 15 of the standard function start register in the DPM and is controlled by the host system. The cons state bit is bit 15 of the standard function status register in the DPM and is controlled by the IBS USC4-2.

Phase A

This phase corresponds to "asynchronous" mode without optionally locking access to the process image.

The process image is updated by the IBS USC4-2 in the DPM synchronously with the cycle. As the host system accesses the process image asynchronously, it cannot be ensured that all of the IN data read by the host system comes from one INTERBUS data cycle or that all of the OUT data provided by the host system is transmitted to the I/O devices in one INTERBUS data cycle.

Phase B

The host system uses the 0→1 edge of the cons activate bit to indicated that is wants to read IN data or write OUT data that is consistent in terms of time.

Once the IBS USC4-2 has detected this edge, it completes the update procedure of the process image for the last IBS cycle. It then uses the 0→1 edge of the cons state bit to indicate that it will no longer access the process image.

In this phase, the host system waits for the 0→1 edge of the cons state bit.

Phase C

In this phase, the IBS USC4-2 does not access the process image. This means that all of the IN data in the process image is from the last INTERBUS data cycle.

The host system can now solely access the process image and thus receives the entire consistent process image of the IN data from the last INTERBUS data cycle, which was executed before the cons activate bit was set.

In this phase, the host system must also write its OUT data to the process image.

Once the process image has been processed completely, the host system resets the cons activate bit.

Phase D

In this phase, the host system must no longer modify the OUT data of the process image, as data transmission to the I/O devices in one INTERBUS data cycle could not be ensured.

After detecting the 1→0 edge of the cons activate bit the IBS USC4-2 has unrestricted access to the process image.

Once the OUT data has been accepted by the IBS USC4-2, the IBS USC4-2 resets the cons state bit. However, this does not mean that the OUT data has been transmitted to the I/O devices without error.

4.4.1 Programming

The protocol used in "asynchronous mode with consistency locking" can be enabled and disabled by the host system at any time. No specific initialization is required. Interrupts from and to the IBS USC4-2 are not implemented.

When using the protocol, please note that the cons state bit is no longer operated by the IBS USC4-2 in the event of an INTERBUS data cycle stop (triggered by an error or a service). For this reason, the application on the host system must monitor the INTERBUS activity (e.g., by evaluating the master diagnostic status register) when waiting for an edge change of the cons state bit.

The programming versions described below differ as follows:

– In version 1 the last valid IN data is read. Then the OUT data for the next INTERBUS data cycle is written.
– In version 2 the OUT data is written first. After OUT data transmission the IN data is read upon the next INTERBUS data cycle.

4.4.2 Examples for Driver Routines

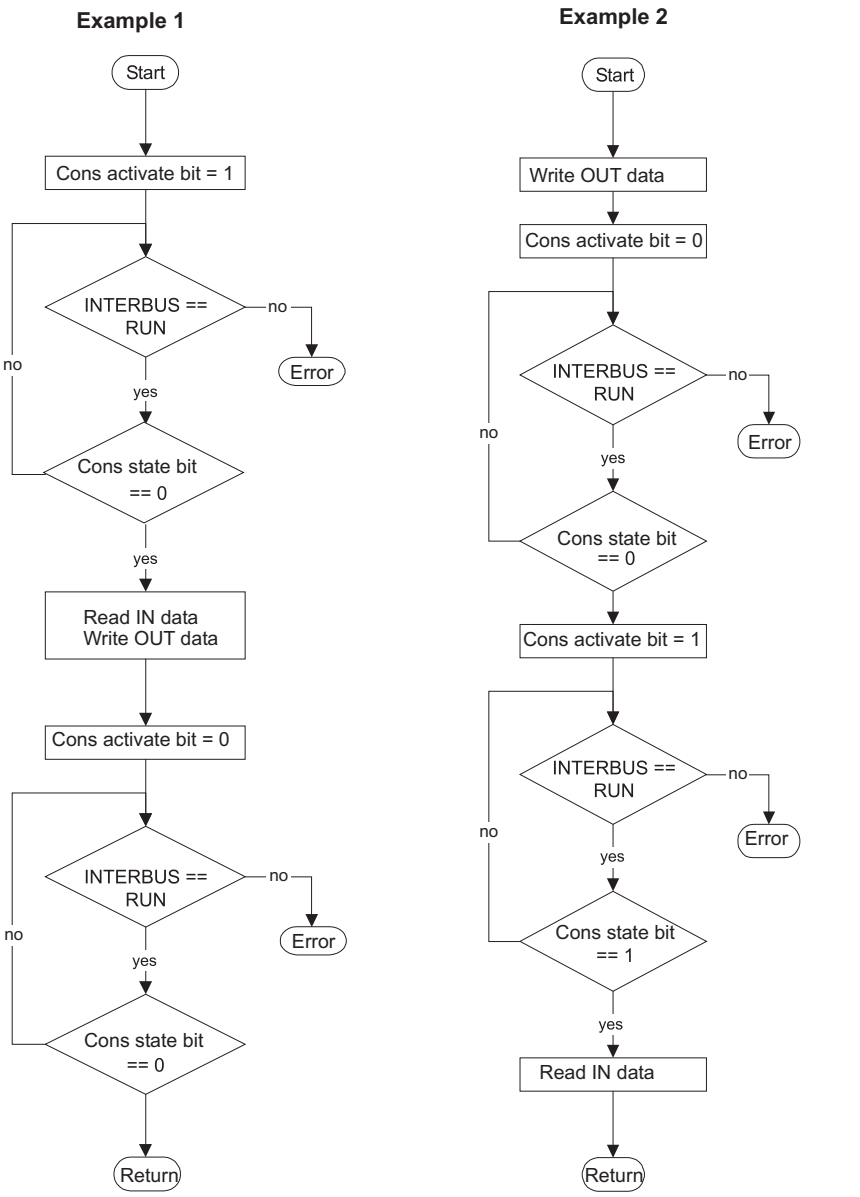


Figure 4-8 Implementation of the "asynchronous mode with consistency locking"

4.5 Asynchronous Data Exchange With Sychronization Pulse

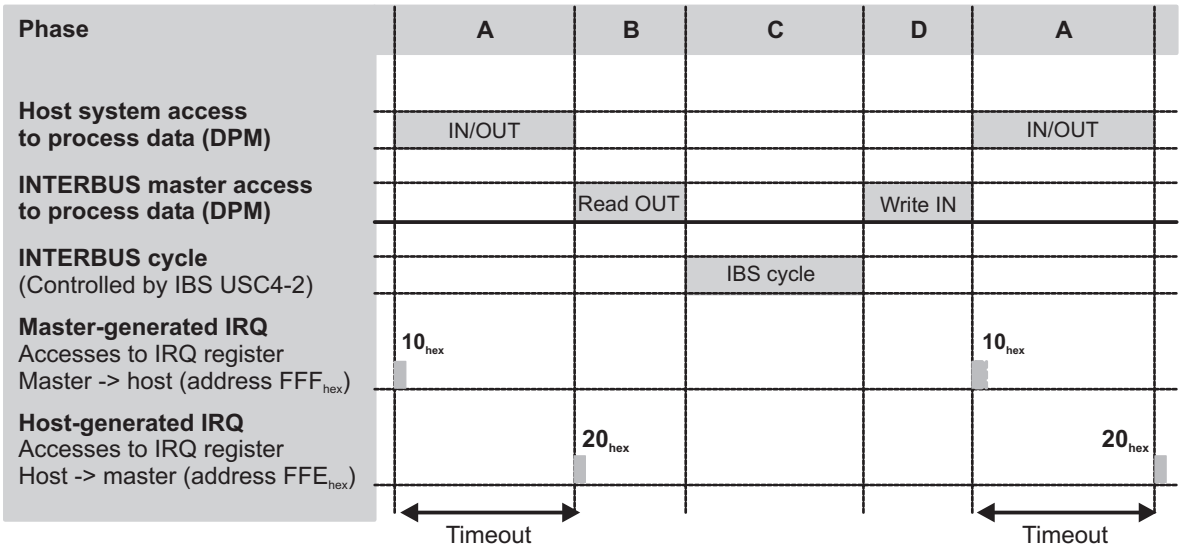


Figure 4-9 Access to the process image in "asynchronous mode with synchronization pulse"

Prior to starting process data cycles using the "Start_Data_Transfer_Request" firmware service, "asynchronous mode with synchronization pulse" must be set (see Section 4.5.2 on page 4-16). The operating principle of this mode is shown in Figure 4-9.

After finishing an INTERBUS cycle and updating the process data in the DPM, the INTERBUS master triggers an interrupt in the direction of the host system by writing the value 10_{hex} to the relevant interrupt register in the DPM. This starts phase A (Figure 4-9).

Phase A

The application can now access the DPM, which contains consistent process data. The host system then triggers an interrupt in the direction of the IBS USC4-2 by entering the value 20_{hex} to the interrupt register. This starts phase B.

The INTERBUS master firmware monitors phase A in order to respond to any malfunctions in the host system. The application must trigger a counter interrupt in the direction of the master within half of the bus timeout (By default, this application

timeout is set to 100 ms provided that, by default, the bus timeout is set to 200 ms.). If the time is exceeded the IBS USC4-2 stops data communication on INTERBUS and reports a synchronization error (BDE_{hex}).

Phase B After receiving the interrupt from the application, the INTERBUS master reads the OUT data in the DPM and prepares the next INTERBUS cycle.

Phase C The IBS USC4-2 carries out an INTERBUS cycle.

Phase D After the INTERBUS cycle has been finished, the IBS USC4-2 writes new IN data to the corresponding area in the DPM. An interrupt is then triggered again in the direction of the application by entering the value 10_{hex} in the IRQ register (master host) in the DPM. This restarts phase A (Figure 4-10).

4.5.1 Programming

"Asynchronous mode with synchronization pulse" is activated with variable ID 2200_{hex} before starting INTERBUS using the Set_Value service (750_{hex}) (see Section 4.5.2, "Setting the Operating Mode").

In the event of an INTERBUS data cycle stop (triggered by an error or a firmware service) the interrupt handshake mechanism is no longer operated by the IBS USC4-2. For this reason, the host system must monitor the INTERBUS activity (e.g., by evaluating the master diagnostic status register) when waiting for an interrupt.

4.5.2 Setting the Operating Mode

The settings required for this operating mode are specified using the Set_Value service and variable ID 200_{hex} (Table 4-2).

Table 4-2 Structure of the Set_Value service for controlling the synchronization pulse

Set_Value_Request code	0750_{hex}
Number of parameters	0004_{hex}
Number of subsequent variable IDs	0001_{hex}
Variable ID	2200_{hex}
Value (0600_{hex}: **ON**; 0000_{hex}:**OFF**)	0600_{hex}
Value	0000_{hex}

4.5.3 Implementing Interrupt Mode

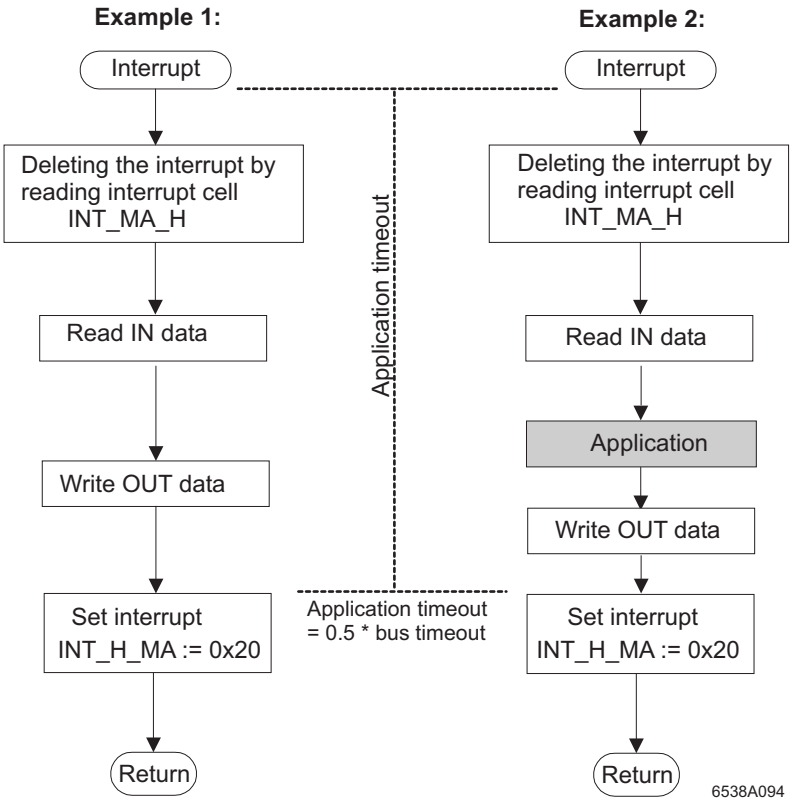


Figure 4-10 Interrupt mode in "asynchronous mode with synchronization pulse"

A Appendices

A 1 List of Figures

Section 2

Section 3

Section 4

A 2 List of Tables

Section 2

Section 4

A 3 Index

O

P

R

S

T

V

W

We Are Interested in Your Opinion!

We would like to hear your comments and suggestions concerning this document.

We review and consider all comments for inclusion in future documentation.

Please fill out the form on the following page and fax it to us or send your comments, suggestions for improvement, etc. to the following address:

Phoenix Contact GmbH & Co. KG
Marketing Services
Dokumentation INTERBUS
32823 Blomberg
GERMANY

Phone +49 - (0) 52 35 - 3-00
Telefax +49 - (0) 52 35 - 3-4 18 08
E-Mail tecdoc@phoenixcontact.com

FAX Reply

Phoenix Contact GmbH & Co. KG
Marketing Services
Dokumentation INTERBUS

Date: _____

Fax No: +49 - (0) 52 35 - 3-4 18 08

From:

Company:		Name:	
		Department:	
Address:		Job function:	
City, ZIP code:		Phone:	
Country:		Fax:	

Document:

Designation: IBS USC4-2 Revision: 01 Order No.: _____

My Opinion on the Document

Form	**Yes**	**In part**	**No**
Is the table of contents clearly arranged?	☐	☐	☐
Are the figures/diagrams easy to understand/helpful?	☐	☐	☐
Are the written explanations of the figures adequate?	☐	☐	☐
Does the quality of the figures meet your expectations/needs?	☐	☐	☐
Does the layout of the document allow you to find information easily?	☐	☐	☐
Contents	**Yes**	**In part**	**No**
Is the phraseology/terminology easy to understand?	☐	☐	☐
Are the index entries easy to understand/helpful?	☐	☐	☐
Are the examples practice-oriented?	☐	☐	☐
Is the document easy to handle?	☐	☐	☐
Is any important information missing? If yes, what?	☐	☐	☐

Other Comments: