

## SCH3223 Silicon Errata and Data Sheet Clarification

**TABLE 1: SILICON DEV/REV VALUES**

Part Number	Device ID <sup>(1)</sup>	Revision ID for Silicon Revision <sup>(2)</sup>
		A
SCH3223	7Dh	02h

**Note 1:** The Device ID is visible as an 8-bit number at Plug and Play Configuration Index 20h.  
**Note 2:** The HW Revision Number is visible as an 8-bit number at Plug and Play Configuration Index 21h and Version/Stepping Number Register 3Fh.

**TABLE 2: SILICON ISSUE SUMMARY**

Module	Feature	Item Number	Issue Summary	Affected Revisions <sup>(1)</sup>
				A
none	none	none	There are no current silicon issues.	

**Note 1:** If there are multiple revision-letter columns under this one, only those issues indicated in the last column apply to the current silicon revision.

## Data Sheet Clarifications

**Note:** The following typographic corrections and clarifications apply only to the SCH3223 Data Sheet, which is currently Document #00002028B. Other members of the SCH322x family have separate data sheets, and separate errata sheets.

**TABLE 3: DATA SHEET CLARIFICATION SUMMARY**

Module	Item Number	Issue Summary
Temp Monitor and Fan Control	1.	No Support for HWM SMI Events
Power Control	2.	32KHz Clock Required for PB_IN# and PB_OUT#
Programmable Clock Output	3.	Misleading Label in Figure
Temp Monitor and Fan Control	4.	Incorrect Values in Table
Temp Monitor and Fan Control	5.	No Hardware Monitor Interrupt Event on SERIRQ
Runtime Registers	6.	Inconsistent Default for Runtime Registers
LPC Timing Diagrams	7.	Inconsistent PCI Clock Max Period
Serial Ports	8.	References to Non-Existent Serial Port Pins
KBC (Non-Existent)	9.	References to Non-Existent Keyboard Controller

### 1. Module: Temperature Monitoring and Fan Control

The section "Interrupt as an SMI Event," is incorrect. Hardware monitoring interrupts are not routed to the SMI block and do not generate SMI events. The section will be removed in its entirety.

### 2. Module: Power Control Features

A clock is required on CLKI32 (pin 99) to clock in and debounce PB\_IN# and to assert PB\_OUT#. If CLKI32 is either not connected or is not connected to an active clock, PB\_OUT# will not be asserted. CLKI32 should be connected to a 32KHz clock. A clock can be provided for PB\_IN# by connecting CLKI32 to the SUSCLK output from the core logic south bridge.

### 3. Module: Programmable Clock Output

In the figure "Reset Generation Circuit", there is a signal labeled "RESETB". The figure implies that the signal comes in from an input pin. This is incorrect. The figure should indicate that the signal is an internally generated Power On Reset signal.

### 4. Module: Temperature Monitoring and Fan Control

The Nominal Voltage and Maximum Voltage numbers in the table "Voltage Limits vs. Register Setting" are incorrect for the row labeled 2.5V. The table indicates the nominal voltage is 5.0V and the maximum voltage is 6.64V. These two values are incorrect.

The correct nominal voltage is 2.5V, matching the signal name. The maximum voltage is 3.32V.

### 5. Module: Temperature Monitoring and Fan Control

In the subsection titled "Interrupt Event on Serial IRQ", in chapter "Temperature Monitoring and Fan Control", it is stated that the interrupt can be routed to the SERIRQ using configuration register 0x70 in Logical Device A. This is not correct. The Hardware Monitor Interrupt cannot be directly routed to a SERIRQ and there is no configuration register 0x70 in Logical Device A. This subsection will be deleted in subsequent releases of the data sheet.

As described in the subsections that precede this one, the Hardware Monitor interrupt can be routed onto a pin, onto an SMI or onto a PME. If it is required to route the HWM interrupt to a SERIRQ, it can be routed to an SMI, which can in turn be routed on SERIRQ2.

## 6. Module: Runtime Registers

The default POR values listed in the tables "Runtime Register POR Summary" and "Detailed Runtime Register Description" have some errors and inconsistencies.

- The register GP4, at Offset 4E hex, is actually reset to the value 05 hex on VTR POR. Both tables currently give incorrect values for this.

Reserved register locations should not be accessed. However, for the sake of interpreting register dumps, there are the following errata regarding initial contents:

- The Reserved register at Offset 13 hex is reset to the value 44 hex. The tables are currently inconsistent.
- The Reserved register at Offset 10 hex is reset to the value 00 hex, and this happens on every VTR POR (not just on VBAT POR).

## 7. Module: LPC Timing Diagrams

In the chapter "Timing Diagrams", under "LPC Interface Timing", the PCI Clock Period is given an incorrect Maximum value of 33.3ns. It should instead be 52.6ns, which represents the lowest guaranteed LPC frequency of 19MHz.

## 8. Module: References to Non-Existent Serial Port Pins

In multiple places there are references to pins belonging to non-existent Serial Ports; for example TXD3, TXD6. These extra UARTs are features of some other SCH322x Family members, but not the SCH3223, and can be ignored.

## 9. Module: References to Non-Existent Keyboard Controller

In the figure "Power Control Block Diagram", there are references to a "Keyboard Controller". This is a feature of some other SCH322x Family members, but not the SCH3223, and can be ignored.

# SCH3223

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## APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level and Date	Description
DS80000696A (04-11-16)	Initial Draft Version

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ISBN: 9781522404743

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