S-5715 Series

HIGH-SPEED / MIDDLE-SPEED LOW CURRENT CONSUMPTION BOTH POLES / UNIPOLAR DETECTION TYPE HALL IC

www.ablic.com

Rev.2.3_02

The S-5715 Series, developed by CMOS technology, is a high-accuracy Hall IC that operates with high-speed / middle-speed detection and low current consumption.
The output voltage changes when the S-5715 Series detects the intensity level of flux density. Using the S-5715 Series with a magnet makes it possible to detect the open / close and rotation state in various devices.
High-density mounting is possible by using the small SOT-23-3 or the super-small SNT-4A packages.
Due to its high-accuracy magnetic characteristics, the S-5715 Series can make operation's dispersion in the system combined with magnet smaller.

Caution **This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to ABLIC Inc. is indispensable.**

■ Features

- Pole detection[*1]: Detection of both poles, S pole or N pole
- Detection logic for magnetism[*1]: Active "L", active "H"
- Output form[*1]: Nch open-drain output, CMOS output
- Magnetic sensitivity: B_{OP} = 3.0 mT typ.
- Operating cycle (current consumption)[*1]:
  Product with both poles detection
  t_{CYCLE} = 0.10 ms (1400 μA) typ.
  t_{CYCLE} = 0.90 ms (155 μA) typ.
  t_{CYCLE} = 5.70 ms (26 μA) typ.
  Product with S pole or N pole detection
  t_{CYCLE} = 0.05 ms (1400 μA) typ.
  t_{CYCLE} = 1.25 ms (60 μA) typ.
  t_{CYCLE} = 6.05 ms (13 μA) typ.
- Power supply voltage range: V_{DD} = 2.7 V to 5.5 V
- Operation temperature range: Ta = −40°C to +85°C
- Lead-free (Sn 100%), halogen-free[*2]

***1**. The option can be selected.
***2**. Refer to "■ **Product Name Structure**" for details.

■ Applications

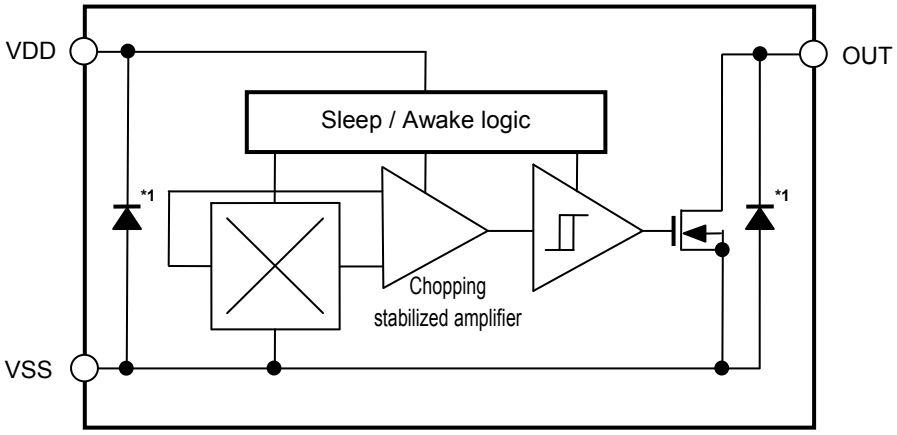
- Plaything, portable game
- Home appliance
- Housing equipment
- Industrial equipment

■ Packages

- SOT-23-3
- SNT-4A

■ Block Diagrams

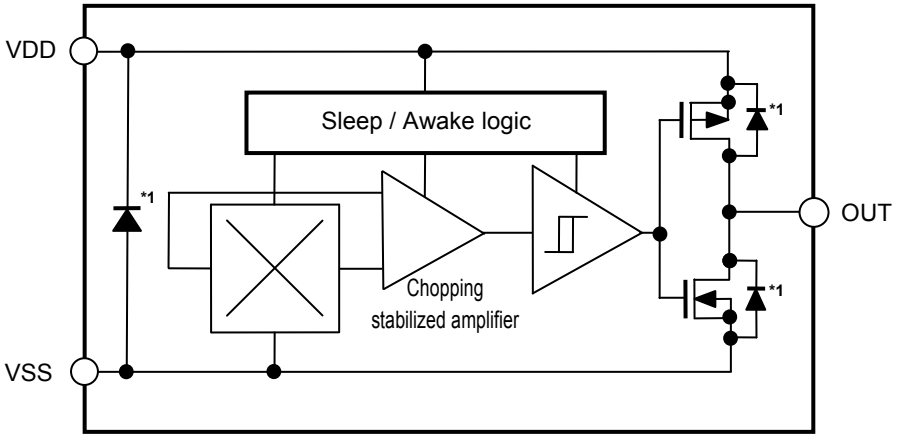
1. Nch open-drain output product



***1.** Parasitic diode

Figure 1

2. CMOS output product

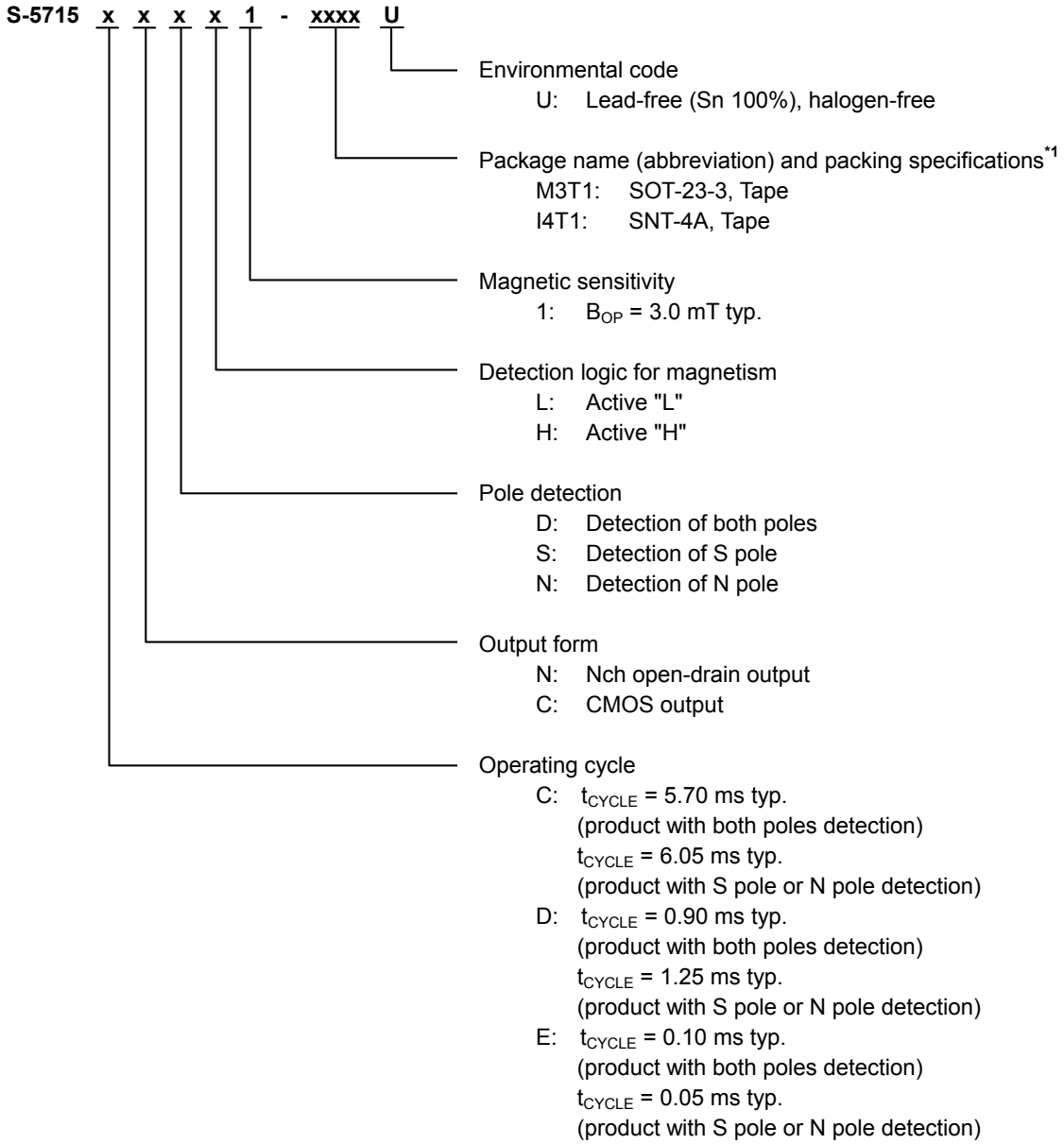


***1.** Parasitic diode

Figure 2

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SOT-23-3	MP003-C-P-SD	MP003-C-C-SD	MP003-Z-R-SD	–
SNT-4A	PF004-A-P-SD	PF004-A-C-SD	PF004-A-R-SD	PF004-A-L-SD

3. Product name list

3. 1 SOT-23-3

3. 1. 1 Nch open-drain output product

Table 2

Product Name	Operating Cycle (t_{CYCLE})	Output Form	Pole Detection	Detection Logic for Magnetism	Magnetic Sensitivity (B_{OP})
S-5715CNDL1-M3T1U	5.70 ms	Nch open-drain output	Both poles	Active "L"	3.0 mT typ.
S-5715CNSL1-M3T1U	6.05 ms	Nch open-drain output	S pole	Active "L"	3.0 mT typ.
S-5715DNDL1-M3T1U	0.90 ms	Nch open-drain output	Both poles	Active "L"	3.0 mT typ.
S-5715DNSL1-M3T1U	1.25 ms	Nch open-drain output	S pole	Active "L"	3.0 mT typ.
S-5715ENDL1-M3T1U	0.10 ms	Nch open-drain output	Both poles	Active "L"	3.0 mT typ.
S-5715ENSL1-M3T1U	0.05 ms	Nch open-drain output	S pole	Active "L"	3.0 mT typ.
S-5715ENSH1-M3T1U	0.05 ms	Nch open-drain output	S pole	Active "H"	3.0 mT typ.

Remark Please contact our sales office for products other than the above.

3. 1. 2 CMOS output product

Table 3

Product Name	Operating Cycle (t_{CYCLE})	Output Form	Pole Detection	Detection Logic for Magnetism	Magnetic Sensitivity (B_{OP})
S-5715CCDL1-M3T1U	5.70 ms	CMOS output	Both poles	Active "L"	3.0 mT typ.
S-5715CCSL1-M3T1U	6.05 ms	CMOS output	S pole	Active "L"	3.0 mT typ.
S-5715DCDL1-M3T1U	0.90 ms	CMOS output	Both poles	Active "L"	3.0 mT typ.
S-5715DCSL1-M3T1U	1.25 ms	CMOS output	S pole	Active "L"	3.0 mT typ.
S-5715ECDL1-M3T1U	0.10 ms	CMOS output	Both poles	Active "L"	3.0 mT typ.
S-5715ECSL1-M3T1U	0.05 ms	CMOS output	S pole	Active "L"	3.0 mT typ.

Remark Please contact our sales office for products other than the above.

3. 2 SNT-4A

3. 2. 1 Nch open-drain output product

Table 4

Product Name	Operating Cycle (t_{CYCLE})	Output Form	Pole Detection	Detection Logic for Magnetism	Magnetic Sensitivity (B_{OP})
S-5715CNDL1-I4T1U	5.70 ms	Nch open-drain output	Both poles	Active "L"	3.0 mT typ.
S-5715CNSL1-I4T1U	6.05 ms	Nch open-drain output	S pole	Active "L"	3.0 mT typ.
S-5715CNNL1-I4T1U	6.05 ms	Nch open-drain output	N pole	Active "L"	3.0 mT typ.
S-5715DNDL1-I4T1U	0.90 ms	Nch open-drain output	Both poles	Active "L"	3.0 mT typ.
S-5715DNSL1-I4T1U	1.25 ms	Nch open-drain output	S pole	Active "L"	3.0 mT typ.
S-5715ENDL1-I4T1U	0.10 ms	Nch open-drain output	Both poles	Active "L"	3.0 mT typ.

Remark Please contact our sales office for products other than the above.

3. 2. 2 CMOS output product

Table 5

Product Name	Operating Cycle (t_{CYCLE})	Output Form	Pole Detection	Detection Logic for Magnetism	Magnetic Sensitivity (B_{OP})
S-5715CCDL1-I4T1U	5.70 ms	CMOS output	Both poles	Active "L"	3.0 mT typ.
S-5715CCSL1-I4T1U	6.05 ms	CMOS output	S pole	Active "L"	3.0 mT typ.
S-5715CCNL1-I4T1U	6.05 ms	CMOS output	N pole	Active "L"	3.0 mT typ.
S-5715DCDL1-I4T1U	0.90 ms	CMOS output	Both poles	Active "L"	3.0 mT typ.
S-5715DCSL1-I4T1U	1.25 ms	CMOS output	S pole	Active "L"	3.0 mT typ.
S-5715ECDL1-I4T1U	0.10 ms	CMOS output	Both poles	Active "L"	3.0 mT typ.

Remark Please contact our sales office for products other than the above.

■ Pin Configurations

1. SOT-23-3

Top view

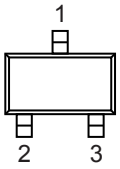


Figure 3

Table 6

Pin No.	Symbol	Description
1	VSS	GND pin
2	VDD	Power supply pin
3	OUT	Output pin

2. SNT-4A

Top view

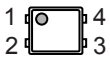


Figure 4

Table 7

Pin No.	Symbol	Description
1	VDD	Power supply pin
2	VSS	GND pin
3	NC*1	No connection
4	OUT	Output pin

***1.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

■ Absolute Maximum Ratings

Table 8

(Ta = +25°C unless otherwise specified)

Item		Symbol	Absolute Maximum Rating	Unit
Power supply voltage		V_{DD}	V_{SS} − 0.3 to V_{SS} + 7.0	V
Output current		I_{OUT}	±2.0	mA
Output voltage	Nch open-drain output product	V_{OUT}	V_{SS} − 0.3 to V_{SS} + 7.0	V
	CMOS output product		V_{SS} − 0.3 to V_{DD} + 0.3	V
Power dissipation	SOT-23-3	P_D	430[*1]	mW
	SNT-4A		300[*1]	mW
Operation ambient temperature		T_{opr}	−40 to +85	°C
Storage temperature		T_{stg}	−40 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

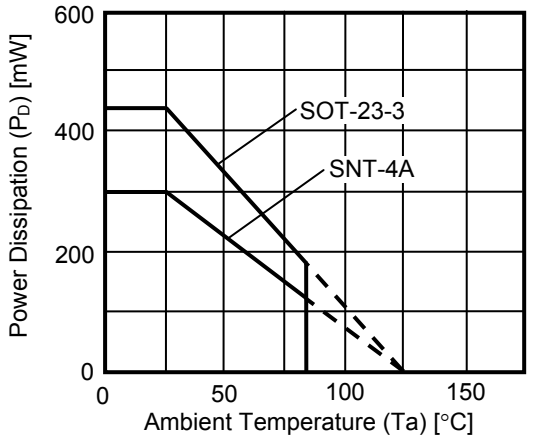


Figure 5 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

1. Product with both poles detection

1. 1 S-5715CxDxx

Table 9

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–		2.7	5.0	5.5	V	–
Current consumption	I_{DD}	Average value		–	26.0	40.0	μA	1
Output voltage	V_{OUT}	Nch open-drain output product	Output transistor Nch, I_{OUT} = 2 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I_{OUT} = 2 mA	–	–	0.4	V	2
			Output transistor Pch, I_{OUT} = −2 mA	V_{DD} − 0.4	–	–	V	3
Leakage current	I_{LEAK}	Nch open-drain output product Output transistor Nch, V_{OUT} = 5.5 V		–	–	1	μA	4
Awake mode time	t_{AW}	–		–	0.10	–	ms	–
Sleep mode time	t_{SL}	–		–	5.60	–	ms	–
Operating cycle	t_{CYCLE}	t_{AW} + t_{SL}		–	5.70	12.00	ms	–

1. 2 S-5715DxDxx

Table 10

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–		2.7	5.0	5.5	V	–
Current consumption	I_{DD}	Average value		–	155.0	230.0	μA	1
Output voltage	V_{OUT}	Nch open-drain output product	Output transistor Nch, I_{OUT} = 2 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I_{OUT} = 2 mA	–	–	0.4	V	2
			Output transistor Pch, I_{OUT} = −2 mA	V_{DD} − 0.4	–	–	V	3
Leakage current	I_{LEAK}	Nch open-drain output product Output transistor Nch, V_{OUT} = 5.5 V		–	–	1	μA	4
Awake mode time	t_{AW}	–		–	0.10	–	ms	–
Sleep mode time	t_{SL}	–		–	0.80	–	ms	–
Operating cycle	t_{CYCLE}	t_{AW} + t_{SL}		–	0.90	2.00	ms	–

1. 3 S-5715ExDxx

Table 11

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–		2.7	5.0	5.5	V	–
Current consumption	I_{DD}	Average value		–	1400.0	2000.0	μA	1
Output voltage	V_{OUT}	Nch open-drain output product	Output transistor Nch, I_{OUT} = 2 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I_{OUT} = 2 mA	–	–	0.4	V	2
			Output transistor Pch, I_{OUT} = −2 mA	V_{DD} − 0.4	–	–	V	3
Leakage current	I_{LEAK}	Nch open-drain output product Output transistor Nch, V_{OUT} = 5.5 V		–	–	1	μA	4
Awake mode time	t_{AW}	–		–	0.10	–	ms	–
Sleep mode time	t_{SL}	–		–	0.00	–	ms	–
Operating cycle	t_{CYCLE}	t_{AW} + t_{SL}		–	0.10	0.20	ms	–

2. Product with S pole or N pole detection

2. 1 S-5715CxSxx, S-5715CxNxx

Table 12

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–		2.7	5.0	5.5	V	–
Current consumption	I_{DD}	Average value		–	13.0	20.0	μA	1
Output voltage	V_{OUT}	Nch open-drain output product	Output transistor Nch, I_{OUT} = 2 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I_{OUT} = 2 mA	–	–	0.4	V	2
			Output transistor Pch, I_{OUT} = −2 mA	V_{DD} − 0.4	–	–	V	3
Leakage current	I_{LEAK}	Nch open-drain output product Output transistor Nch, V_{OUT} = 5.5 V		–	–	1	μA	4
Awake mode time	t_{AW}	–		–	0.05	–	ms	–
Sleep mode time	t_{SL}	–		–	6.00	–	ms	–
Operating cycle	t_{CYCLE}	t_{AW} + t_{SL}		–	6.05	12.00	ms	–

2. 2 S-5715DxSxx, S-5715DxNxx

Table 13

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–		2.7	5.0	5.5	V	–
Current consumption	I_{DD}	Average value		–	60.0	90.0	μA	1
Output voltage	V_{OUT}	Nch open-drain output product	Output transistor Nch, I_{OUT} = 2 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I_{OUT} = 2 mA	–	–	0.4	V	2
			Output transistor Pch, I_{OUT} = −2 mA	V_{DD} − 0.4	–	–	V	3
Leakage current	I_{LEAK}	Nch open-drain output product Output transistor Nch, V_{OUT} = 5.5 V		–	–	1	μA	4
Awake mode time	t_{AW}	–		–	0.05	–	ms	–
Sleep mode time	t_{SL}	–		–	1.20	–	ms	–
Operating cycle	t_{CYCLE}	t_{AW} + t_{SL}		–	1.25	2.50	ms	–

2. 3 S-5715ExSxx, S-5715ExNxx

Table 14

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–		2.7	5.0	5.5	V	–
Current consumption	I_{DD}	Average value		–	1400.0	2000.0	μA	1
Output voltage	V_{OUT}	Nch open-drain output product	Output transistor Nch, I_{OUT} = 2 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I_{OUT} = 2 mA	–	–	0.4	V	2
			Output transistor Pch, I_{OUT} = −2 mA	V_{DD} − 0.4	–	–	V	3
Leakage current	I_{LEAK}	Nch open-drain output product Output transistor Nch, V_{OUT} = 5.5 V		–	–	1	μA	4
Awake mode time	t_{AW}	–		–	0.05	–	ms	–
Sleep mode time	t_{SL}	–		–	0.00	–	ms	–
Operating cycle	t_{CYCLE}	t_{AW} + t_{SL}		–	0.05	0.10	ms	–

■ Magnetic Characteristics

1. Product with both poles detection

Table 15

($Ta = +25°C$, $V_{DD} = 5.0$ V, $V_{SS} = 0$ V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	–	1.4	3.0	4.0	mT	5
	N pole	B_{OPN}	–	–4.0	–3.0	–1.4	mT	5
Release point*2	S pole	B_{RPS}	–	1.1	2.2	3.7	mT	5
	N pole	B_{RPN}	–	–3.7	–2.2	–1.1	mT	5
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	0.8	–	mT	5
	N pole	B_{HYSN}	$B_{HYSN} = \|B_{OPN} - B_{RPN}\|$	–	0.8	–	mT	5

2. Product with S pole detection

Table 16

($Ta = +25°C$, $V_{DD} = 5.0$ V, $V_{SS} = 0$ V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	–	1.4	3.0	4.0	mT	5
Release point*2	S pole	B_{RPS}	–	1.1	2.2	3.7	mT	5
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	0.8	–	mT	5

3. Product with N pole detection

Table 17

($Ta = +25°C$, $V_{DD} = 5.0$ V, $V_{SS} = 0$ V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	N pole	B_{OPN}	–	–4.0	–3.0	–1.4	mT	5
Release point*2	N pole	B_{RPN}	–	–3.7	–2.2	–1.1	mT	5
Hysteresis width*3	N pole	B_{HYSN}	$B_{HYSN} = \|B_{OPN} - B_{RPN}\|$	–	0.8	–	mT	5

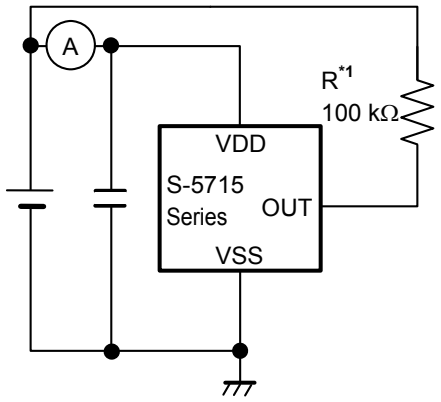
***1.** B_{OPN}, B_{OPS}: Operation points
B_{OPN} and B_{OPS} are the values of magnetic flux density when the output voltage (V_{OUT}) is inverted after the magnetic flux density applied to the S-5715 Series by the magnet (N pole or S pole) is increased (the magnet is moved closer).
Even when the magnetic flux density exceeds B_{OPN} or B_{OPS}, V_{OUT} retains the status.

***2.** B_{RPN}, B_{RPS}: Release points
B_{RPN} and B_{RPS} are the values of magnetic flux density when the output voltage (V_{OUT}) is inverted after the magnetic flux density applied to the S-5715 Series by the magnet (N pole or S pole) is decreased (the magnet is moved further away).
Even when the magnetic flux density falls below B_{RPN} or B_{RPS}, V_{OUT} retains the status.

***3.** B_{HYSN}, B_{HYSS}: Hysteresis widths
B_{HYSN} and B_{HYSS} are the difference between B_{OPN} and B_{RPN}, and B_{OPS} and B_{RPS}, respectively.

Remark The unit of magnetic density mT can be converted by using the formula 1 mT = 10 Gauss.

■ Test Circuits



***1.** Resistor (R) is unnecessary for the CMOS output product.

Figure 6 Test Circuit 1

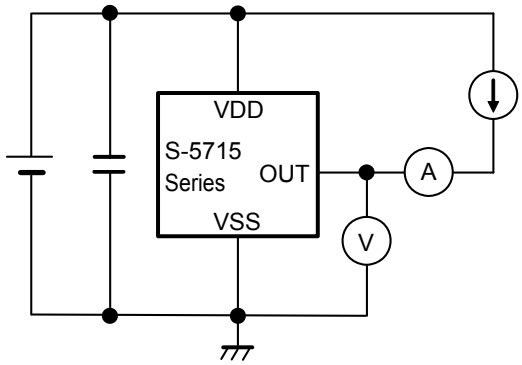


Figure 7 Test Circuit 2

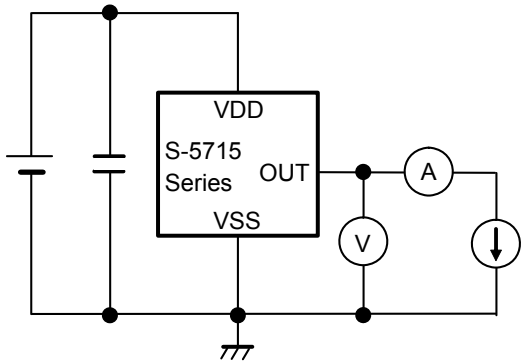


Figure 8 Test Circuit 3

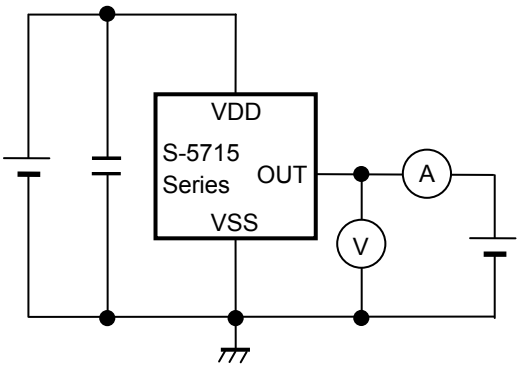
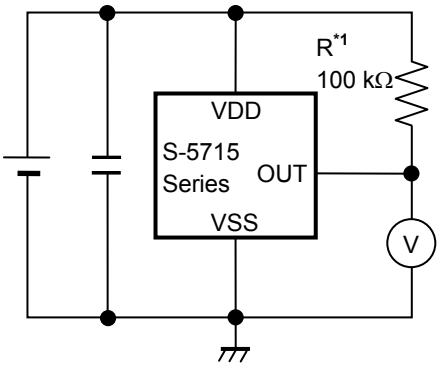


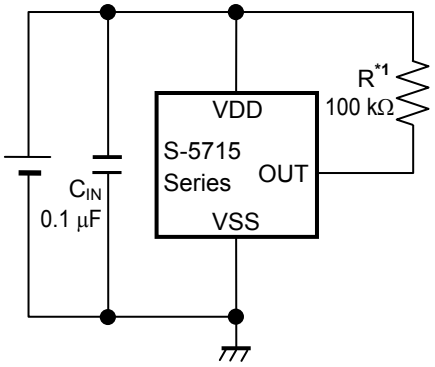
Figure 9 Test Circuit 4



***1.** Resistor (R) is unnecessary for the CMOS output product.

Figure 10 Test Circuit 5

■ Standard Circuit



***1.** Resistor (R) is unnecessary for the CMOS output product.

Figure 11

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

■ Operation

1. Direction of applied magnetic flux

The S-5715 Series detects the flux density which is vertical to the marking surface.
In product with both poles detection, the output voltage (V_{OUT}) is inverted when the S pole or N pole is moved closer to the marking surface.
In product with S pole detection, the output voltage (V_{OUT}) is inverted when the S pole is moved closer to the marking surface.
In product with N pole detection, the output voltage (V_{OUT}) is inverted when the N pole is moved closer to the marking surface.
Figure 12 and **Figure 13** show the direction in which magnetic flux is being applied.

1. 1 SOT-23-3

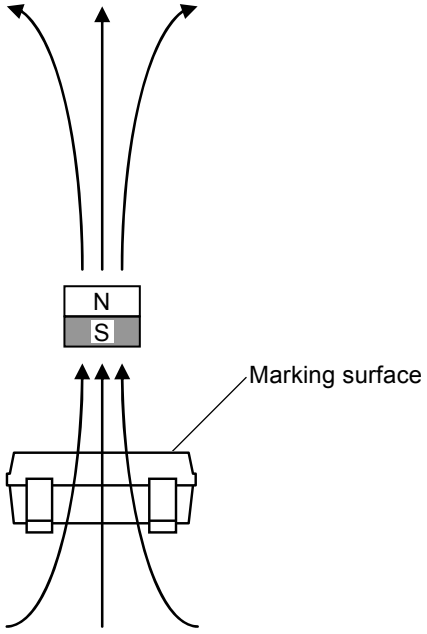


Figure 12

1. 2 SNT-4A

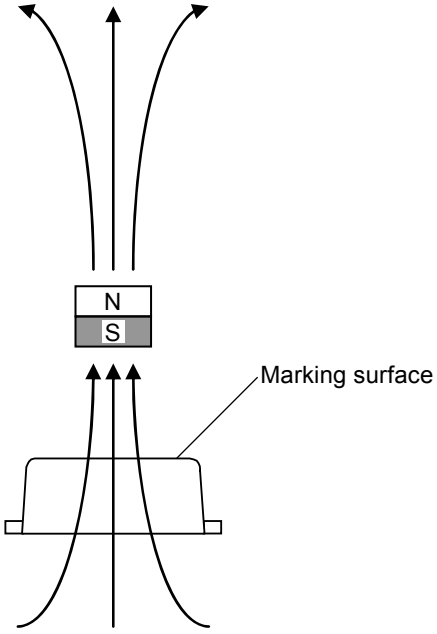


Figure 13

2. Position of Hall sensor

Figure 14 and **Figure 15** show the position of Hall sensor.
The center of this Hall sensor is located in the area indicated by a circle, which is in the center of a package as described below.
The following also shows the distance (typ. value) between the marking surface and the chip surface of a package.

2. 1 SOT-23-3

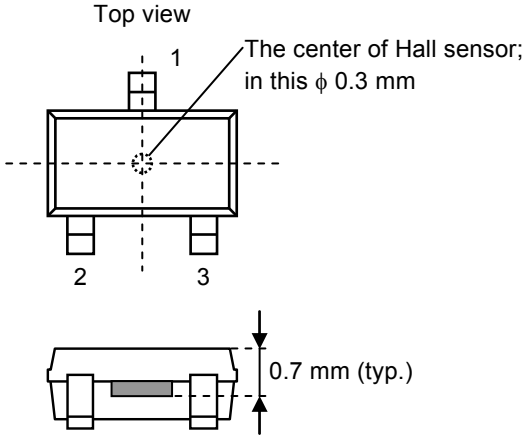


Figure 14

2. 2 SNT-4A

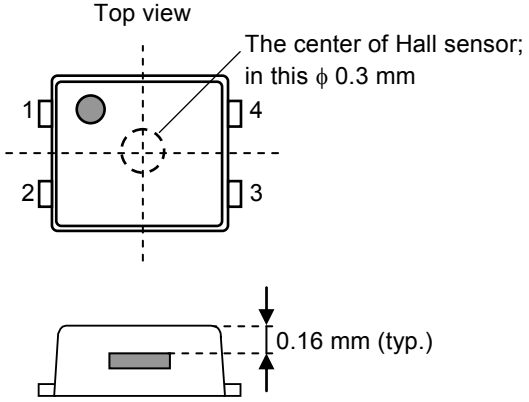


Figure 15

3. Basic operation

The S-5715 Series changes the output voltage level (V_{OUT}) according to the level of the magnetic flux density (N pole or S pole) applied by a magnet.
The following explains the operation when the magnetism detection logic is active "L".

3. 1 Product with both poles detection

When the magnetic flux density vertical to the marking surface exceeds B_{OPN} or B_{OPS} after the S pole or N pole of a magnet is moved closer to the marking surface of the S-5715 Series, V_{OUT} changes from "H" to "L". When the S pole or N pole of a magnet is moved further away from the marking surface of the S-5715 Series and the magnetic flux density is lower than B_{RPN} or B_{RPS}, V_{OUT} changes from "L" to "H".
Figure 16 shows the relationship between the magnetic flux density and V_{OUT}.

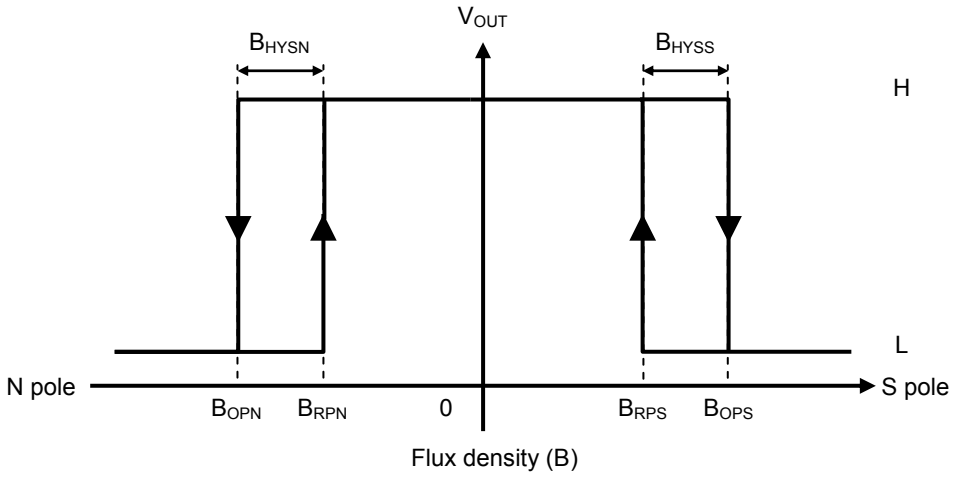


Figure 16

3. 2 Product with S pole detection

When the magnetic flux density vertical to the marking surface exceeds B_{OPS} after the S pole of a magnet is moved closer to the marking surface of the S-5715 Series, V_{OUT} changes from "H" to "L". When the S pole of a magnet is moved further away from the marking surface of the S-5715 Series and the magnetic flux density is lower than B_{RPS}, V_{OUT} changes from "L" to "H".
Figure 17 shows the relationship between the magnetic flux density and V_{OUT}.

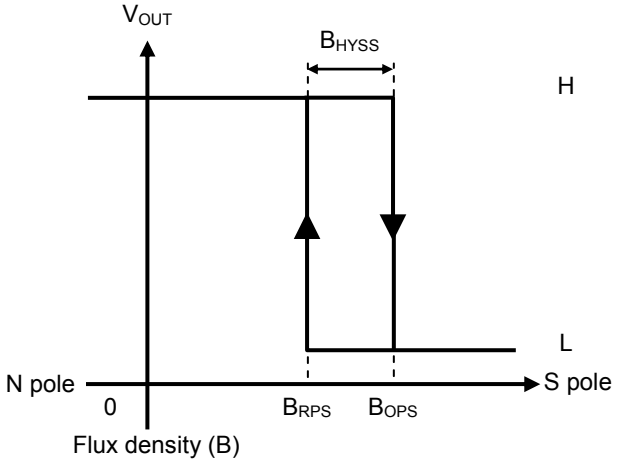


Figure 17

3. 3 Product with N pole detection

When the magnetic flux density vertical to the marking surface exceeds B_{OPN} after the N pole of a magnet is moved closer to the marking surface of the S-5715 Series, V_{OUT} changes from "H" to "L". When the N pole of a magnet is moved further away from the marking surface of the S-5715 Series and the magnetic flux density is lower than B_{RPN}, V_{OUT} changes from "L" to "H".
Figure 18 shows the relationship between the magnetic flux density and V_{OUT}.

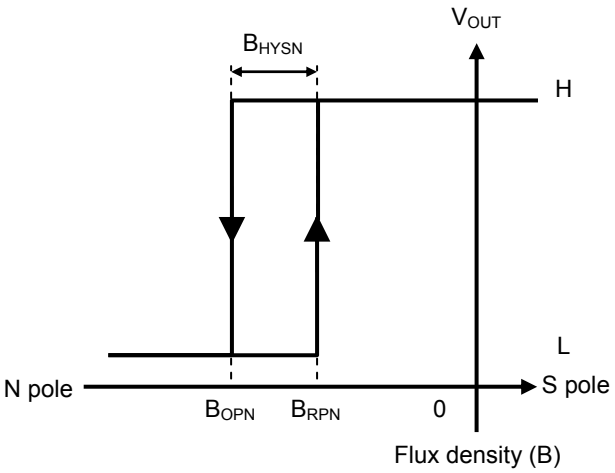


Figure 18

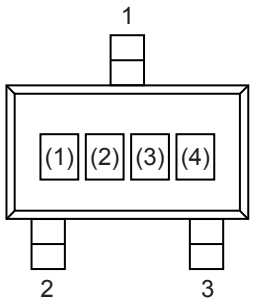
■ Precautions

- If the impedance of the power supply is high, the IC may malfunction due to a supply voltage drop caused by feed-through current. Take care with the pattern wiring to ensure that the impedance of the power supply is low.
- Note that the IC may malfunction if the power supply voltage rapidly changes.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Large stress on this IC may affect on the magnetic characteristics. Avoid large stress which is caused by bend and distortion during mounting the IC on a board or handle after mounting.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Marking Specifications

1. SOT-23-3

Top view



(1) to (3): Product code (Refer to **Product name vs. Product code**.)
(4): Lot number

Product name vs. Product code

1. 1 Nch open-drain output product

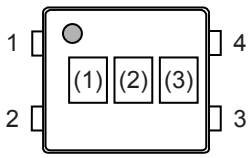
Product Name	Product Code		
	(1)	(2)	(3)
S-5715CNDL1-M3T1U	X	2	C
S-5715CNSL1-M3T1U	X	2	L
S-5715DNDL1-M3T1U	X	2	B
S-5715DNSL1-M3T1U	X	2	O
S-5715ENDL1-M3T1U	X	2	R
S-5715ENSL1-M3T1U	X	2	A
S-5715ENSH1-M3T1U	X	2	U

1. 2 CMOS output product

Product Name	Product Code		
	(1)	(2)	(3)
S-5715CCDL1-M3T1U	X	2	M
S-5715CCSL1-M3T1U	X	2	N
S-5715DCDL1-M3T1U	X	2	P
S-5715DCSL1-M3T1U	X	2	Q
S-5715ECDL1-M3T1U	X	2	S
S-5715ECSL1-M3T1U	X	2	T

2. SNT-4A

Top view



(1) to (3): Product code (Refer to **Product name vs. Product code**.)

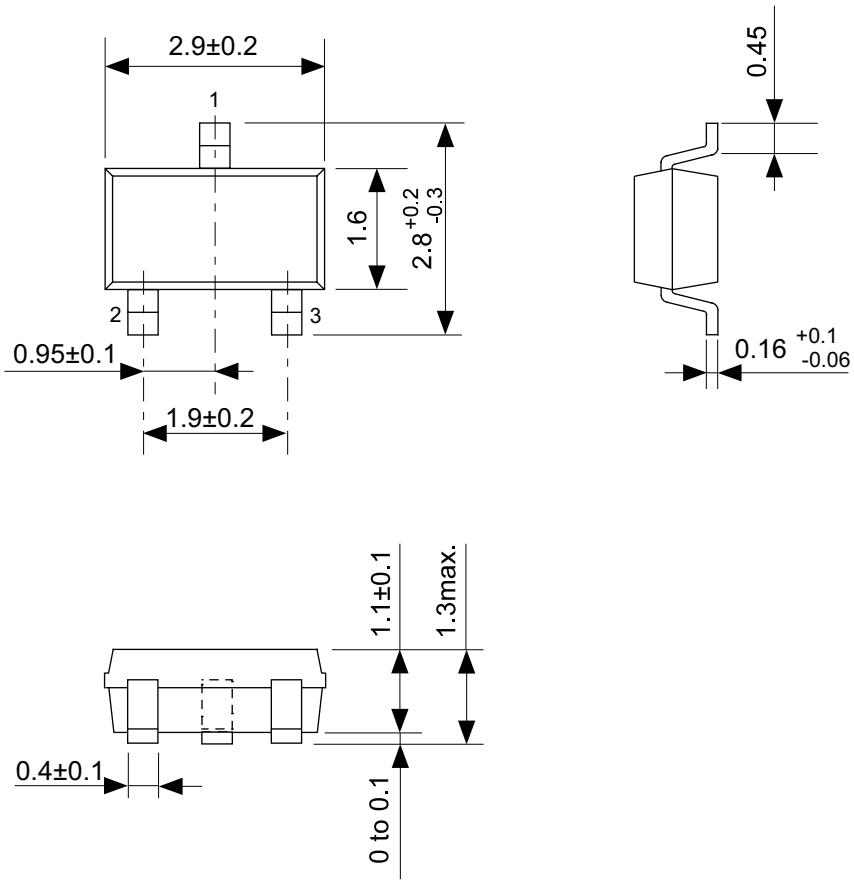
Product name vs. Product code

2. 1 Nch open-drain output product

Product Name	Product Code		
	(1)	(2)	(3)
S-5715CNDL1-I4T1U	X	2	C
S-5715CNSL1-I4T1U	X	2	L
S-5715CNNL1-I4T1U	X	2	V
S-5715DNDL1-I4T1U	X	2	B
S-5715DNSL1-I4T1U	X	2	O
S-5715ENDL1-I4T1U	X	2	R

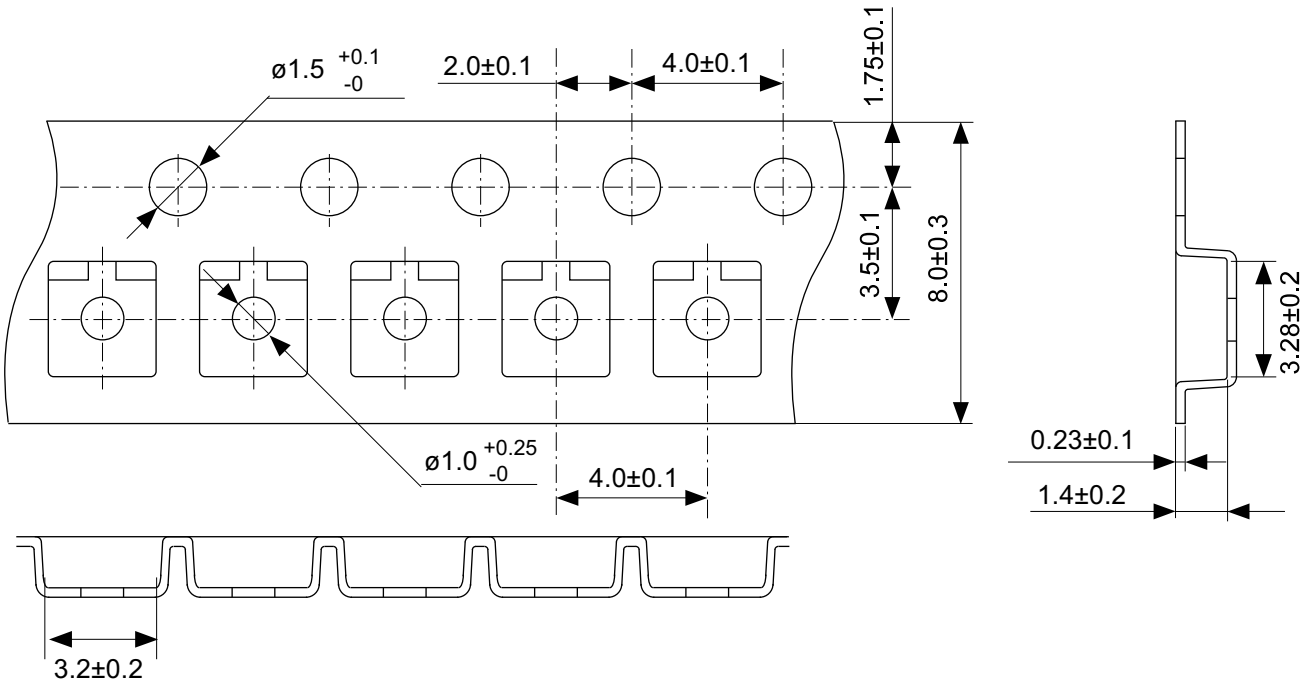
2. 2 CMOS output product

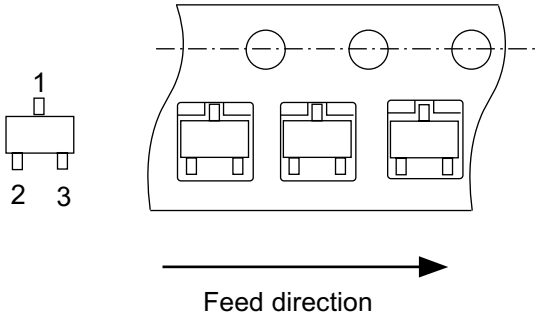
Product Name	Product Code		
	(1)	(2)	(3)
S-5715CCDL1-I4T1U	X	2	M
S-5715CCSL1-I4T1U	X	2	N
S-5715CCNL1-I4T1U	X	2	W
S-5715DCDL1-I4T1U	X	2	P
S-5715DCSL1-I4T1U	X	2	Q
S-5715ECDL1-I4T1U	X	2	S



No. MP003-C-P-SD-1.1

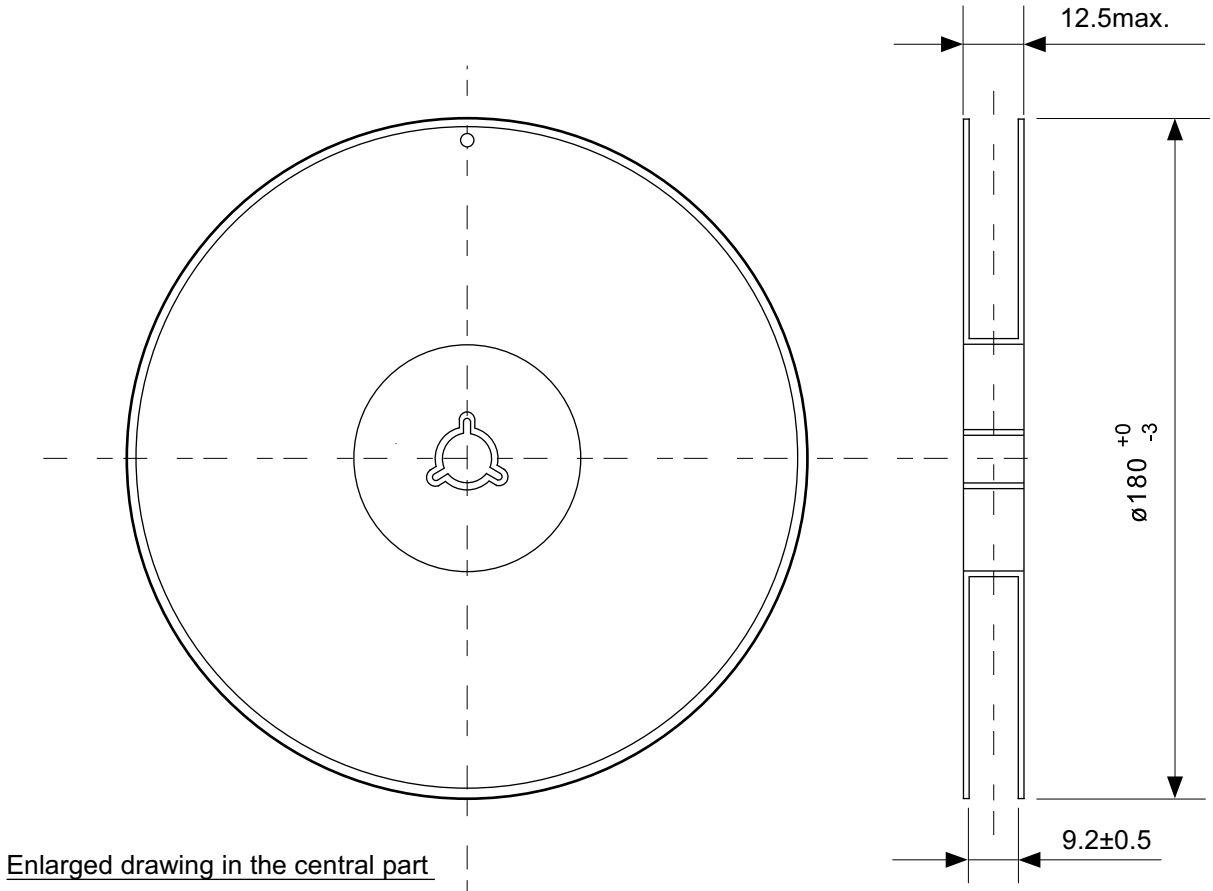
TITLE	SOT233-C-PKG Dimensions
No.	MP003-C-P-SD-1.1
ANGLE	
UNIT	mm
ABLIC Inc.	



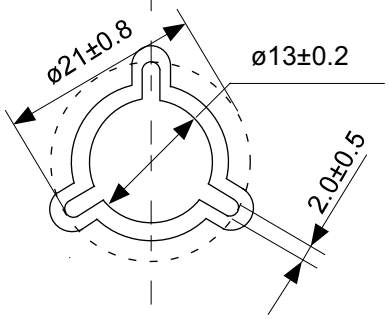


No. MP003-C-C-SD-2.0

TITLE	SOT233-C-Carrier Tape
No.	MP003-C-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

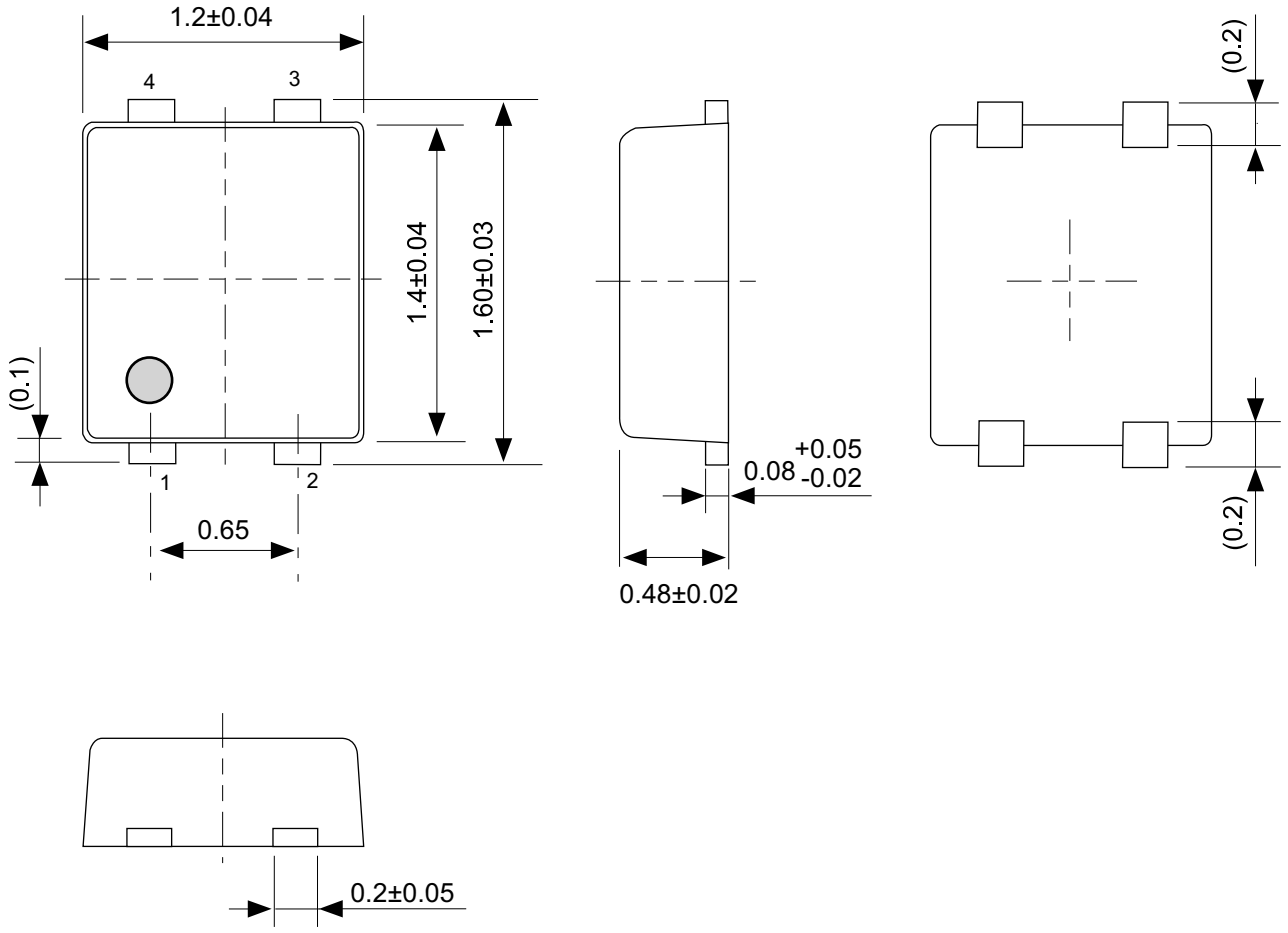


Enlargement drawing in the central part



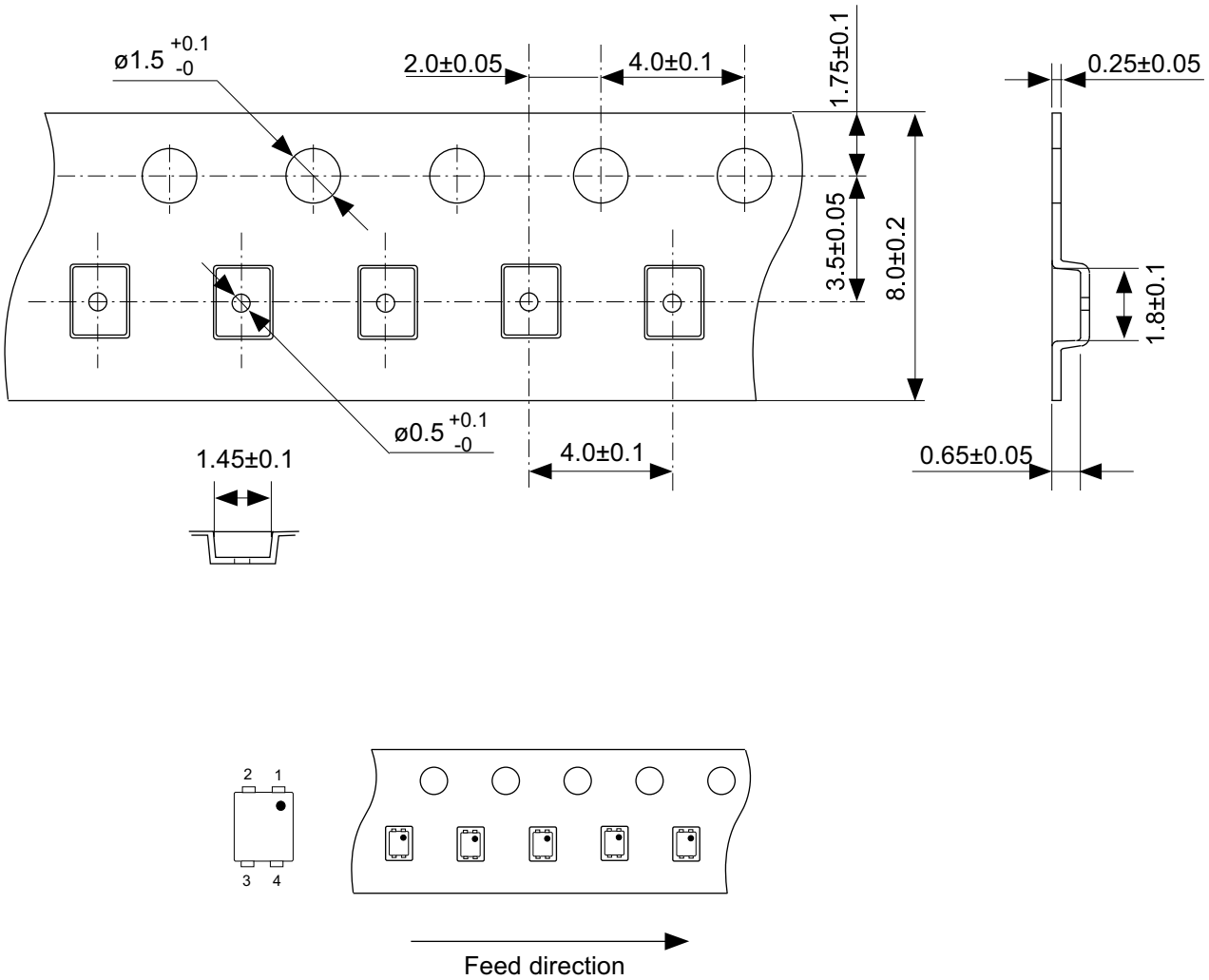
No. MP003-Z-R-SD-1.0

TITLE	SOT233-C-Reel		
No.	MP003-Z-R-SD-1.0		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			



No. PF004-A-P-SD-6.0

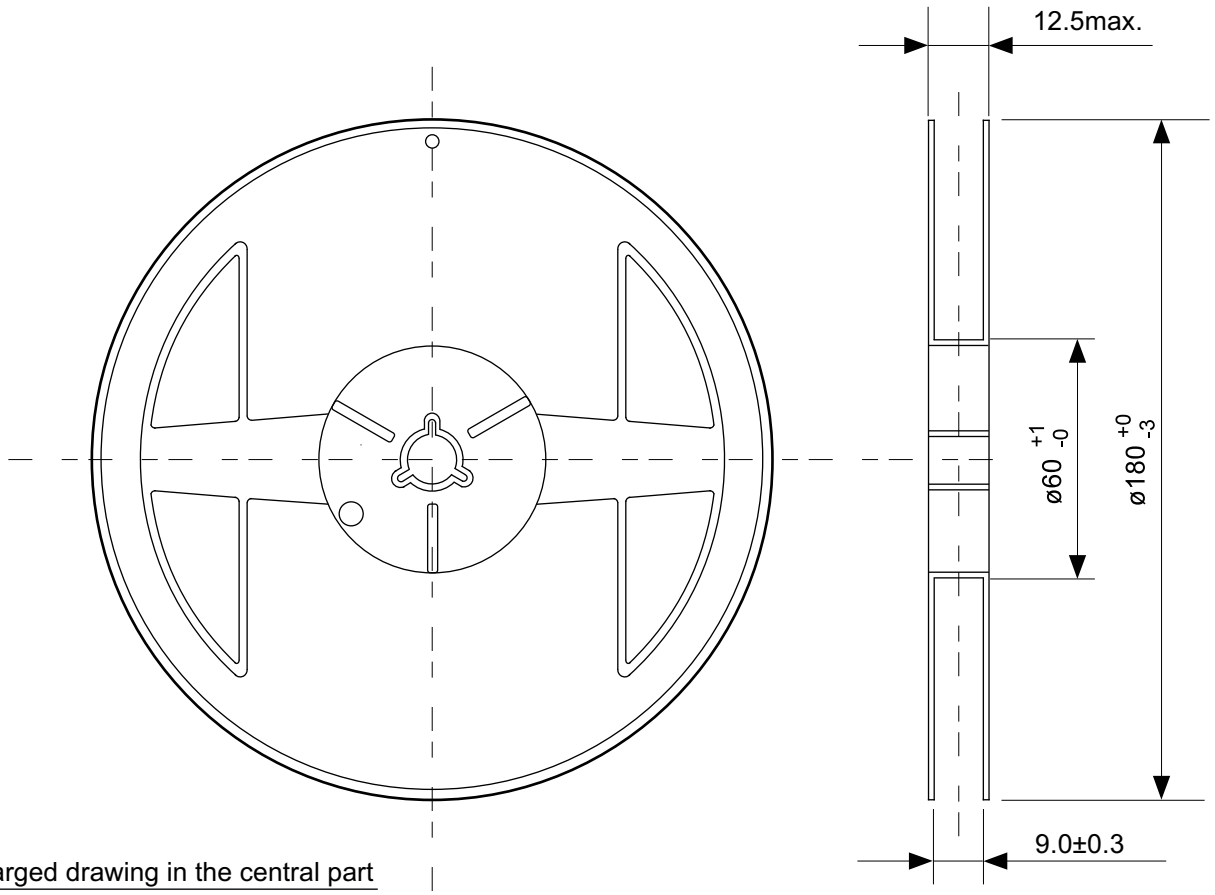
TITLE	SNT-4A-A-PKG Dimensions
No.	PF004-A-P-SD-6.0
ANGLE	
UNIT	mm
ABLIC Inc.	



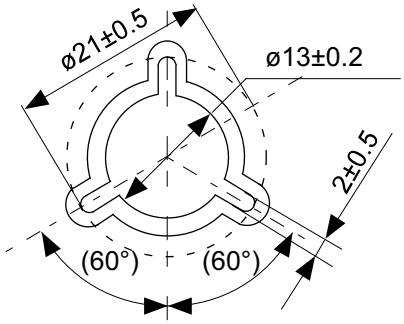
No. PF004-A-C-SD-2.0

TITLE	SNT-4A-A-Carrier Tape
No.	PF004-A-C-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.



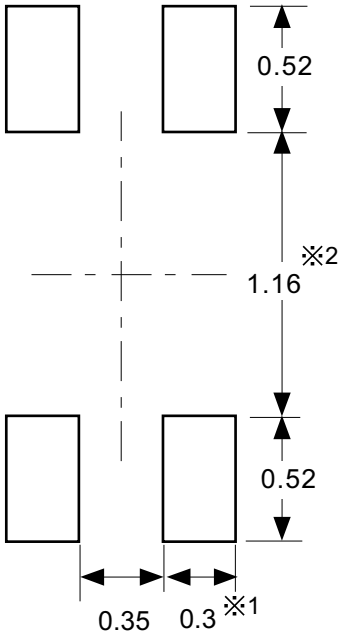
Enlarged drawing in the central part



No. PF004-A-R-SD-1.0

TITLE	SNT-4A-A-Reel		
No.	PF004-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		

ABLIC Inc.



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.10 mm ~ 1.20 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から**0.03 mm** 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は ″SNTパッケージ活用の手引き″ を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.10 mm to 1.20 mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.10 mm ~ 1.20 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PF004-A-L-SD-4.1

TITLE	SNT-4A-A -Land Recommendation
No.	PF004-A-L-SD-4.1
ANGLE	
UNIT	mm

ABLIC Inc.

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2.4-2019.07