PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG-IPC/14/7643
Dated 09 Dec 2014

LNBH29, LNBH29E and LNBH30 : Copper Wire Bonding Implementation on MLP package 3x3 mm and 4x4 mm leads in Carsem (Malaysia)

Table 1. Change Implementation Schedule

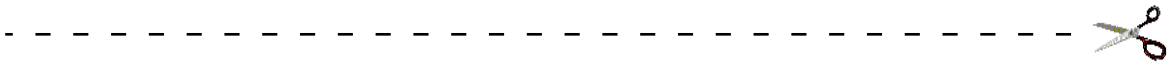
Forecasted implementation date for change	01-Jan-2015
Forecasted availability date of samples for customer	02-Dec-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	15-Dec-2014
Estimated date of changed product first shipment	10-Mar-2015

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	LNBH29, LNBH29E, LNBH30
Type of change	Package assembly material change
Reason for change	To follow the Company guidelines on bonding material implementation
Description of the change	Pad structure (Top Metal) : Ni/Pd layer (3um Nickel / 0.3um Palladium thickness) is added Wire bonding : Copper
Change Product Identification	By a new Finished Goods code
Manufacturing Location(s)	1]Sc Carsem S - Malaysia

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPG-IPC/14/7643**
Please sign and return to STMicroelectronics Sales Office	**Dated 09 Dec 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Pioppo, Sergio Franco	Marketing Manager
Pioppo, Sergio Franco	Product Manager
Moretti, Paolo	Q.A. Manager

ATTACHMENT TO PCN IPD-IPC/13/7643

WHAT*:*
As an extension of the **PCN IPD-IPC/12/7384,** the "Pd/Cu wire bonding on Ni/Pd pad implementation" for BCD6S solutions mounted in MLP package will be adopted and delivered by our subcontractor Carsem located in Malaysia also for the below devices:

LNBH29 (VFDFPN 3x3-16 and VFDFPN 4x4-16)
LNBH29E (VFDFPN 3x3-16 and VFDFPN 4x4-16)
LNBH30 (VFDFPN 4x4-16)

WHY*:*
To comply with the Company requirements for bonding material implementation and to increase delivery flexibility.

HOW*:*
No change in the electrical and mechanical characteristics. Please refer to the Reliability Reports herewith enclosed, related to Carsem, Malaysia (**PCN IPD-IPC/12/7384).**

Three different test vehicles (UM90; UJ58; UJ75) have been checked to guarantee device performance, crossing Front End technologies (BCD6S/BCD6SOI) and Back End package assembly rules with Palladium/copper wire process.

The new process (copper wire) can be traced by the internal part numbers on ST standard labels, as follows:

Commercial Product	New Internal part Number	Back-End Plant
LNBH29PTR	LNBH29PTR$Y4	Carsem Malaysia
LNBH29QTR	LNBH29QTR$Y5	Carsem Malaysia
LNBH29EPTR	LNBH29EPTR$Y3	Carsem Malaysia
LNBH29EQTR	LNBH29EQTR$Y3	Carsem Malaysia
LNBH30QTR	LNBH30QTR$Y4	Carsem Malaysia

WHEN*:*
The change will be implemented starting January, 2015.
Samples are available and can be delivered upon request.

Reliability Evaluation Report

ST8034

New Product Qualification

General Information	
Product Line	*UI87*
Product Description	*Smartcard interfaces*
P/N	*ST8034HNQR* *ST8034PQR* *ST8034ATDT*
Product Group	*AMS*
Product division	*STD Products & HiRel*
Package	*QFN 24L* *QFN 16L* *SO16 narrow*
Silicon Process technology	*BCD6S-3M*

Locations	
Wafer fab	*Catania M5*
Assembly plant	*Carsem S* *QFN 24L* *QFN 16L* *Bouskoura* *SO16 narrow*
Reliability Lab	*Catania Reliability Lab*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	25-Mar-2013	13	A.Riciputo	G.Presti	

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47E	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

New Product, new QFN Package Qualification.

The present evaluation plan includes three different packages for the same product:

QFN 4x4 24L and QFN 3X3-16L packages using CU wires 1 mil, assembled in CARSEM S.

SO16 package packages using CU wires 1 mil, assembled in Bouskoura.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

Smartcard interfaces

4.2 Construction note

	ST8034		
Wafer/Die fab. information			
Wafer fab manufacturing location	Catania M5		
Technology	BCD6S		
Die finishing back side	RAW SILICON		
Die size	1608x1700µm		
Passivation type	TEOS/SiN/Polyimide		
Wafer Testing (EWS) information			
Electrical testing manufacturing location	TPY		
Tester	J750 Teradyne		
Assembly information			
Assembly site	Carsem S		BOUSKOURA
Package description	QFN 4x4 24L	QFN 3x3-16L	SO 16 Narrow
Molding compound	EPOXY		
Wires bonding materials/diameters	Cu 1mil		
Final testing information			
Testing location	Carsem S		BOUSKOURA
Tester	ASL1K		

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Tech. Code	Process/ Package	Product Line	Comments
1	5226598	ENGC3402	AYD8*UI87AA5	BCD6S-3M/ QFN 4x4 24L	UI87	
2		ENGC4003				
3		ENGC3404	AY94*UI87AA5	BCD6S-3M/ QFN 3x3 16L		
4	5226598	LP1249N1P	JDQ7*UI87AA5	BCD6S-3M/ SO16 Narrow		

5.2 Test plan and results summary

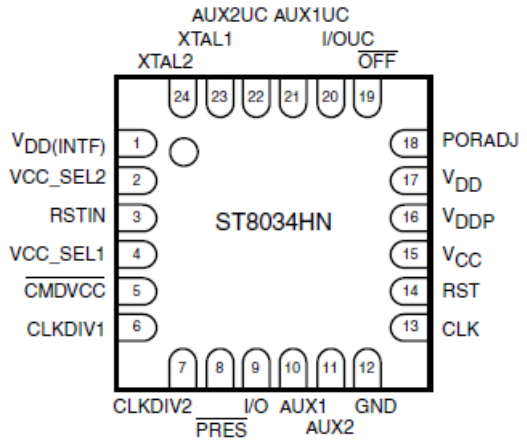
ST8034

Test	PC	Std ref.	Conditions	Steps	Failure/SS				Note
					Lot 1	Lot 2	Lot 3	Lot 4	
Die Oriented Tests									
HTB	N	JESD22 A-108	Tj = 125°C, Vbias=+6V	168 H	0/77				
				500 H	0/77				
				1000 H	0/77				
HTSL	N	JESD22 A-103	Ta = 150°C	168 H	0/45	0/45	0/45	0/45	
				500 H	0/45	0/45	0/45	0/45	
				1000 H	0/45	0/45	0/45	0/45	
Package Oriented Tests									
PC		JESD22 A-113	Drying 24H@125°C Store 168H@Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times	Final	Pass	Pass	Pass	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	96 H	0/77	0/77	0/77	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	100 cy	0/77	0/77	0/77	0/77	
				200 cy	0/77	0/77	0/77	0/77	
				500 cy	0/77	0/77	0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85% Vbias=+5V,	168 H	0/77	0/77		0/77	
				500 H	0/77	0/77		0/77	
				1000 H	0/77	0/77		0/77	
Other Tests									
ESD	N	AEC Q101-001, 002 and 005	HBM	±2KV	Pass			Pass	All pins
				±8KV	Pass			Pass	I/O, RST, VCC, CLK,PRES Pins
			CDM	±500V	Pass	Pass	Pass	Pass	
			MM	±200V	Pass			Pass	
LU	N	AEC Q100 - 004	Current Inj. Overvoltage		Pass			Pass	

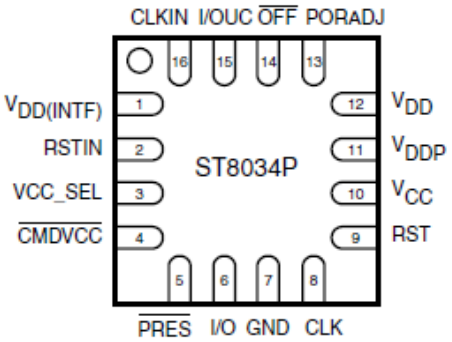
6 ANNEXES

6.1 Device details

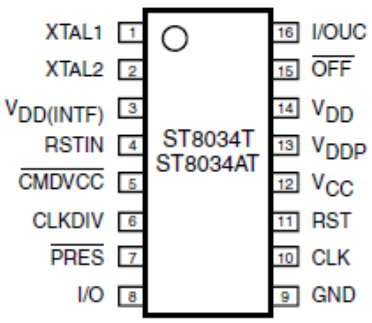
6.1.1 Pin connection



QFN24 - 4 x 4 x 0.8 mm, 0.5 mm pitch

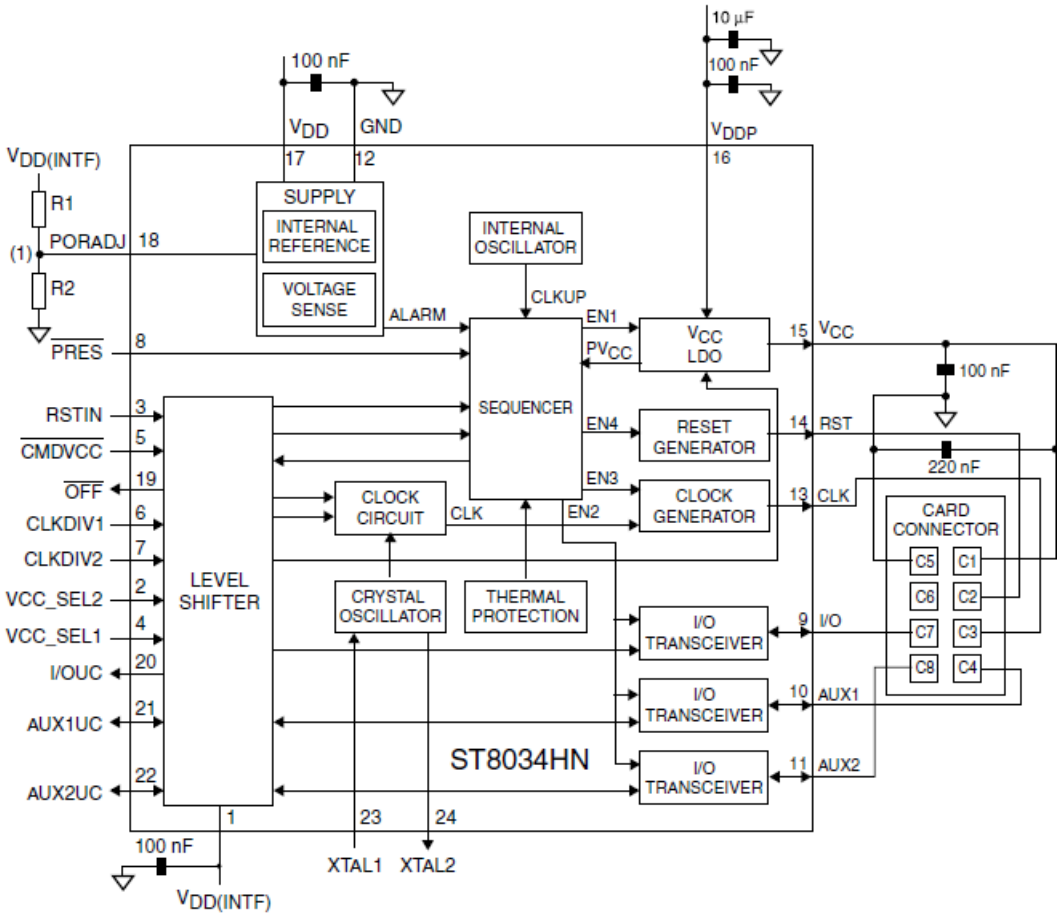


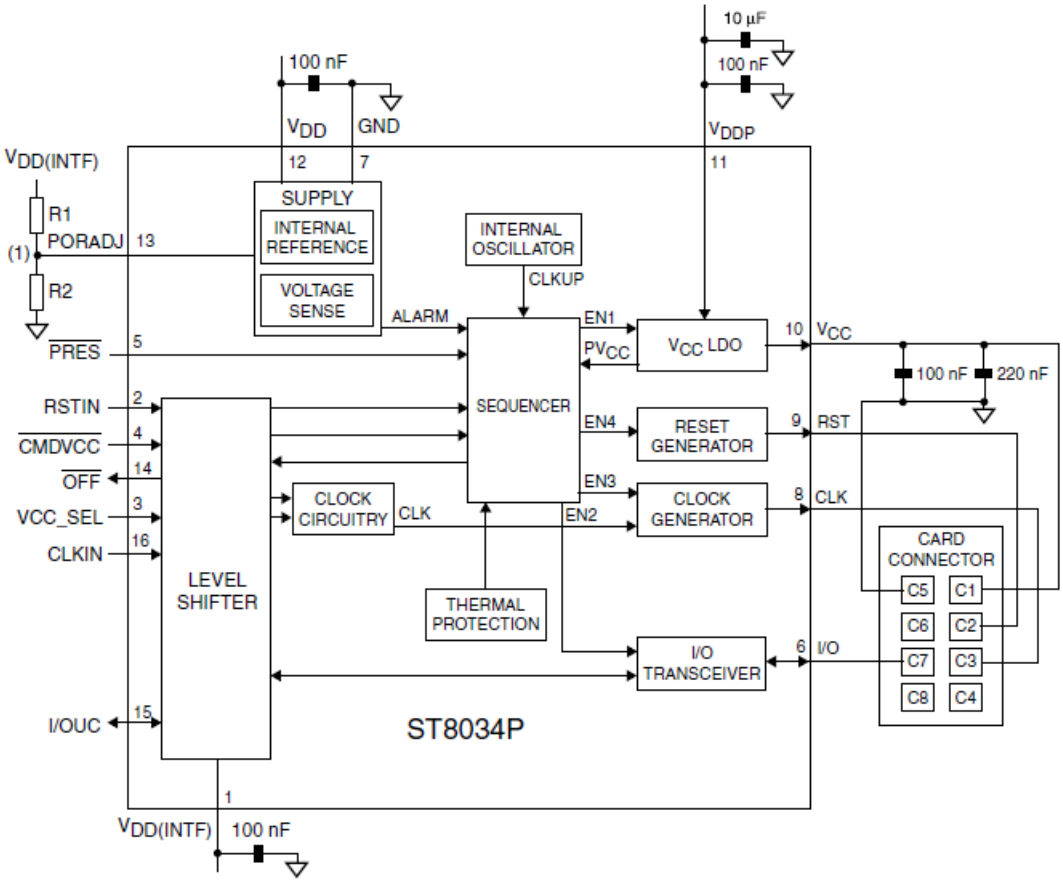
QFN16 3 x 3 x 0.8 mm, 0.5 mm pitch

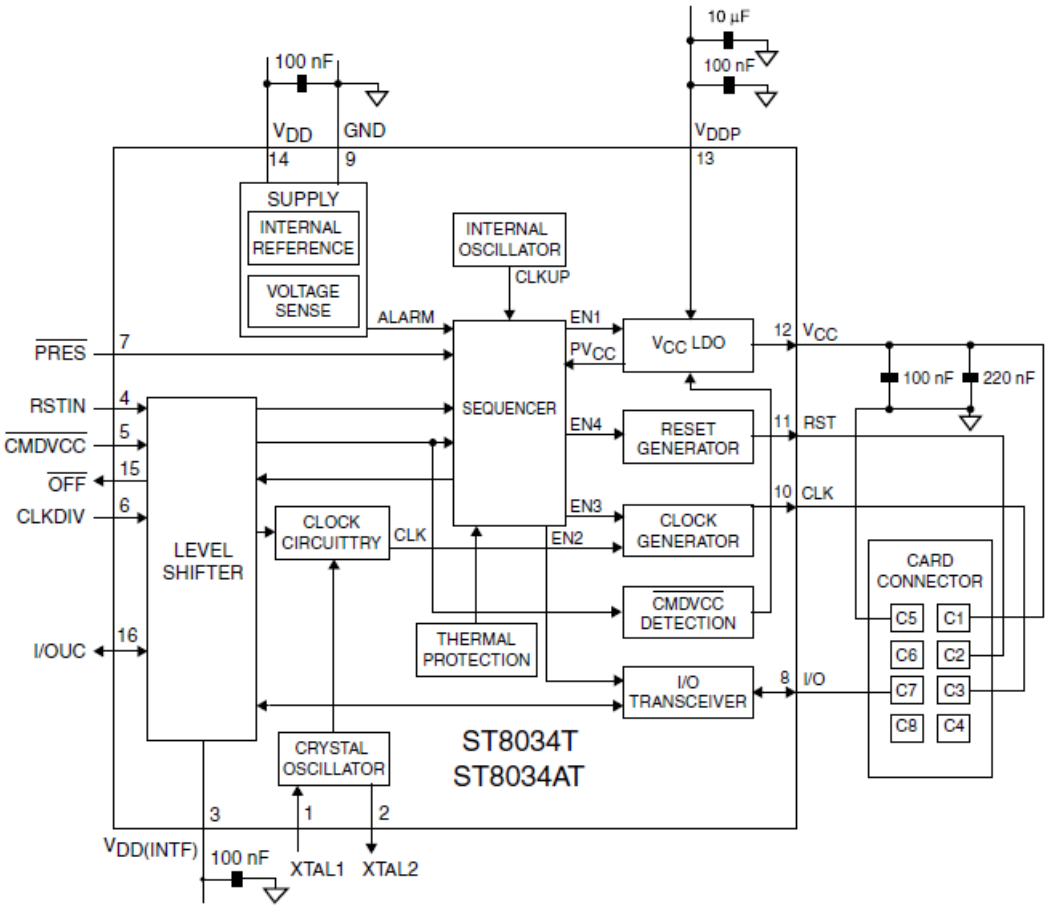


SO16 3.9 x 9.9 mm

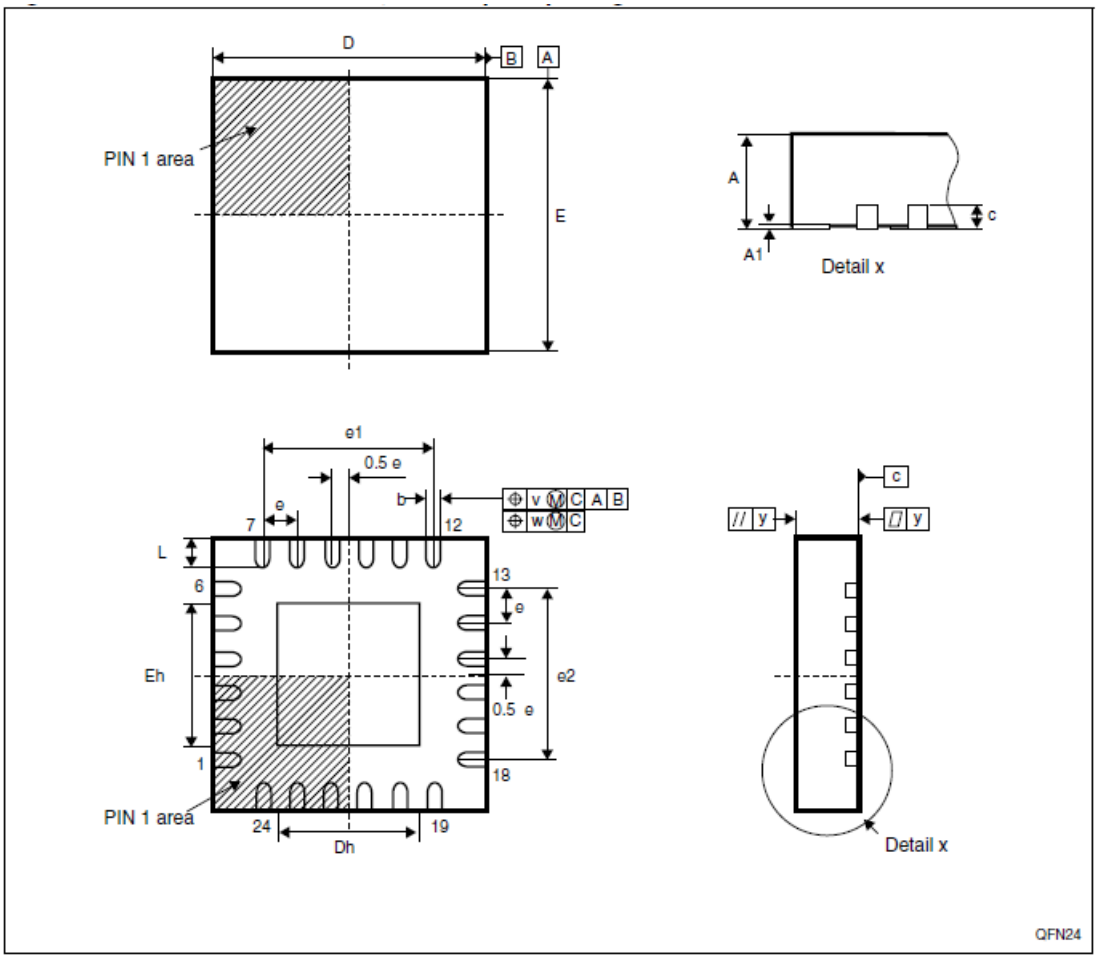
6.1.2 Block diagram



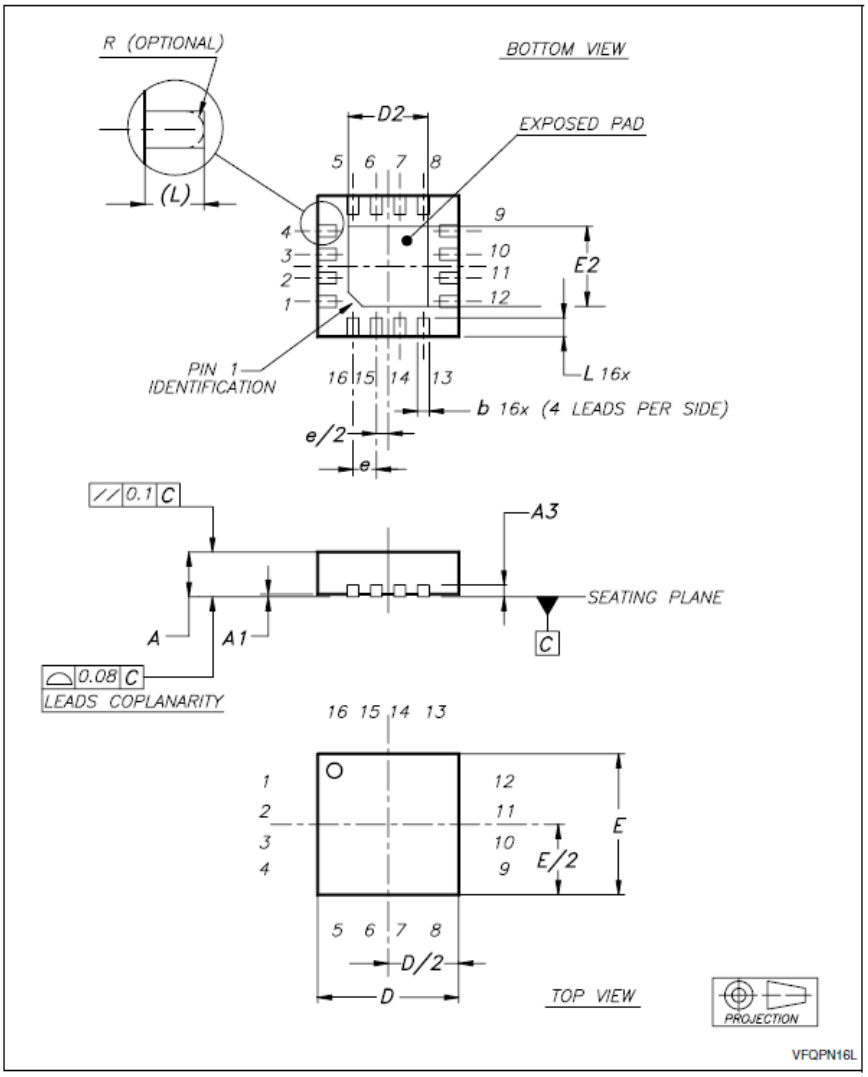

10 µF
100 nF
100 nF
VDD
GND
VDDP
VDD(INTF)
12
7
11
SUPPLY
INTERNAL REFERENCE
VOLTAGE SENSE
INTERNAL OSCILLATOR
CLKUP
R1
PORADJ
13
(1)
R2
ALARM
EN1
PVCC
VCC LDO
10
VCC
PRES
5
100 nF
220 nF
RSTIN
2
SEQUENCER
EN4
RESET GENERATOR
9
RST
CMDVCC
4
OFF
14
EN3
CLOCK GENERATOR
8
CLK
CLOCK CIRCUITRY
CLK
EN2
VCC_SEL
3
CLKIN
16
CARD CONNECTOR
C5
C1
C6
C2
C7
C3
C8
C4
LEVEL SHIFTER
THERMAL PROTECTION
I/O TRANSCEIVER
6
I/O
I/OUC
15
ST8034P
1
VDD(INTF)
100 nF


10 µF
100 nF
100 nF
VDD
GND
VDDP
14
9
13
SUPPLY
INTERNAL REFERENCE
VOLTAGE SENSE
INTERNAL OSCILLATOR
CLKUP
ALARM
EN1
PVCC
VCC LDO
12 VCC
PRES
7
SEQUENCER
100 nF
220 nF
RSTIN
4
EN4
RESET GENERATOR
11 RST
CMDVCC
5
OFF
15
10 CLK
CLKDIV
6
EN3
CLOCK GENERATOR
CLOCK CIRCUITTRY
CLK
EN2
LEVEL SHIFTER
CARD CONNECTOR
C5
C1
C6
C2
C7
C3
C8
C4
CMDVCC DETECTION
THERMAL PROTECTION
I/OUC
16
I/O TRANSCEIVER
8 I/O
CRYSTAL OSCILLATOR
ST8034T
ST8034AT
3
1
2
VDD(INTF)
100 nF
XTAL1
XTAL2

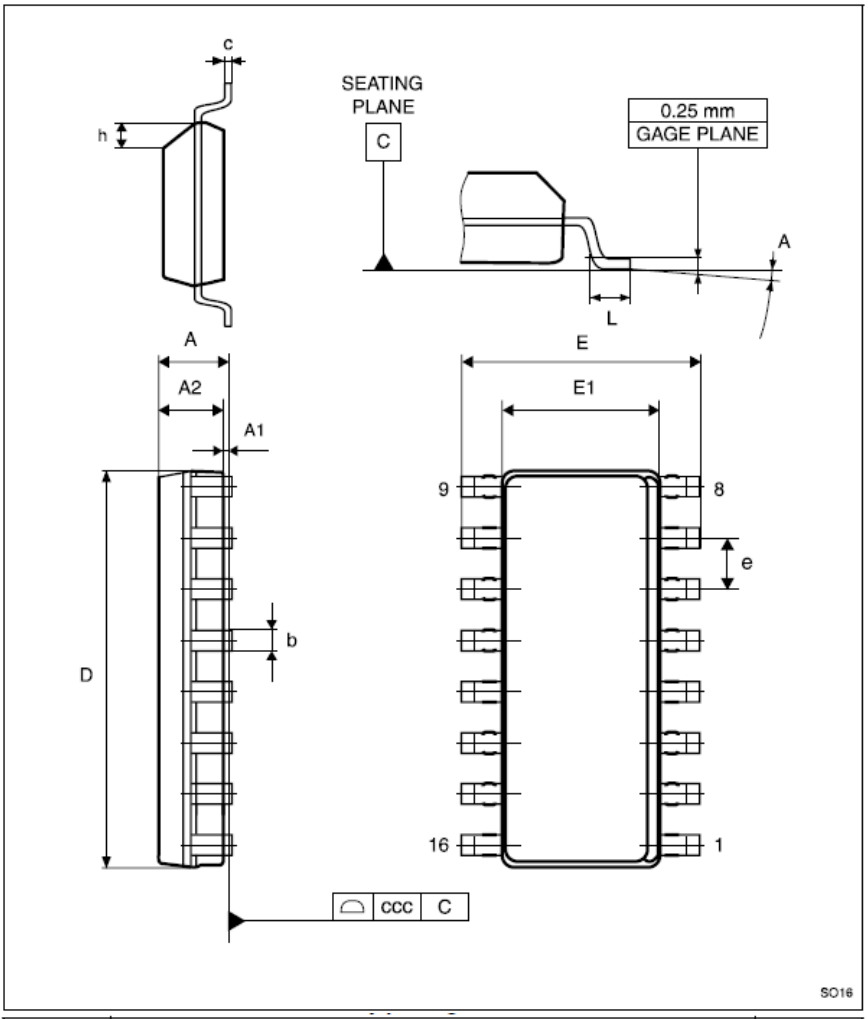
6.1.3 Package outline/Mechanical data



Symbol	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1	Unit
Dim.	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1	mm



Symbol	Dimensions (mm)		
	Nom.	Min.	Max.
A	0.90	0.80	1
A1		0	0.05
A3	0.20		
b		0.18	0.30
D	3	2.90	3.10
D2		1.50	1.80
E	3	2.90	3.10
E2		1.50	1.80
e	0.50		
L		0.30	0.50



Symbol	Dimensions						Notes
	Databook (mm)			Drawing (mm)			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
A			1.75	1.43	1.55	1.68	
A1	0.10		0.25	0.12	0.15	0.18	
A2	1.25			1.48	1.52	1.56	
b	0.31		0.51	0.375	0.40	0.425	
c	0.17		0.25			0.238	
D	9.80	9.90	10.00	9.77	9.80	9.83	(1)
E	5.80	6.00	6.20	5.90	6.00	6.10	
E1	3.80	3.90	4.00	3.82	3.85	3.88	(2)
e		1.27			1.27		
h	0.25		0.50	0.425		0.50	
L	0.40		1.27	0.585	0.635	0.685	(3)
k	0		8	2	4	8	
ccc			0.10			0.04	

6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTB High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CBM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

Reliability Evaluation Report

Cu wires (1,0 mils) - NiPd Pactech Process

Test Vehicles:
LNBH26S-UX68 VFQFPN 4x4x1.0 24L package

General Information	
Product Line	*UX6801*
Product Description	*LNBH26S - Dual LNB power supply*
P/N	LNBH26SPQR
Product Group	*IPD*
Product division	*I3* Handheld & Computer PM
Package	*VFQFPN 4x4x1.0 24L*
Silicon Process technology	*BCD6S*

Locations	
Wafer fab	Catania CTM8
Assembly plant	*Carsem S - Malaysia*
Reliability Lab	*Catania Site*
Reliability assessment	*Pass.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	04-Mar-2013	9	Giuseppe Giacopello	Giovanni Presti	Final

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Reliability evaluation on Cu wires (1,0 mils) on VFDFPN package with PACTECH process

T.V.: UX6801 - LNBH26SPQR

3.2 Conclusion

The final reliability results are positive.

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure).

For HTB and THB test results please refer to the ST8034 device used as test vehicle

4 DEVICE CHARACTERISTICS

4.1 Device description

Intended for analog and digital dual satellite receivers/Sat-TV, and Sat-PC cards, the LNBH26S is a monolithic voltage regulator and interface IC, assembled in QFN24 4x4 specifically designed to provide the 13/18 V power supply and the 22 kHz tone signalling to the LNB downconverter in the antenna dishes or to the multiswitch box. In this application field, it offers a complete solution for dual tuner satellite receivers with extremely low component count, low power dissipation together with simple design and I²C standard interfacing.

4.2 Construction note

	P/N LNBH26S
Wafer/Die fab. information	
Wafer fab manufacturing location	Catania CTM8
Technology	BCD6S
Process family	BCD6 SHRINK
Die finishing back side	Cr/NiV/Au
Die size	2.645 x 2.645 mm2
Bond pad metallization layers	NiPd
Passivation type	TEOS/SiN/Polyimide
Wafer Testing (EWS) information	
Electrical testing manufacturing location	AngMoKio - Singapore
Assembly information	
Assembly site	Carsem S - Malaysia
Package description	VFQFPN 4x4x1.0 24 PITCH 0.5
Molding compound	G770HC
Frame material	MLPQ 4X4 24L expad 118x118 carsem
Die attach material	Epoxy QMI519
Wires bonding materials/diameters	COPPER WIRE 1.0 mil
Lead finishing/bump solder material	Pure tin plating Sn 100%
Final testing information	
Testing location	Carsem S - Malaysia
Tester	ASL1K Credence
Test program	UA29_FT

5 TESTS RESULTS SUMMARY

5.1 Test vehicle(Final Silicon)

Lot #	Assy Lot	Trace Code	Process	Product Line	Comments
1	ENGC4603	RYND*UX68AB5	BCD6S	UX6801	

5.2 Test plan and results summary

P/N LNBH26S

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Note
Die Oriented Tests							
HTSL	N	JESD22 A-103	Ta = 150°C	45	168 h	0/45	
					500 h	0/45	
					1000 h	0/45	
Package Oriented Tests							
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta= 85°C Rh= 85% Over Reflow @ Tpeak= 260°C 3 times		Final	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta= 121°C	77	168 h	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	77	100 cy	0/77	
					200 cy	0/77	
					500 cy	0/77	

Reference: **RER6043-078-W-13**
P/N ST8034

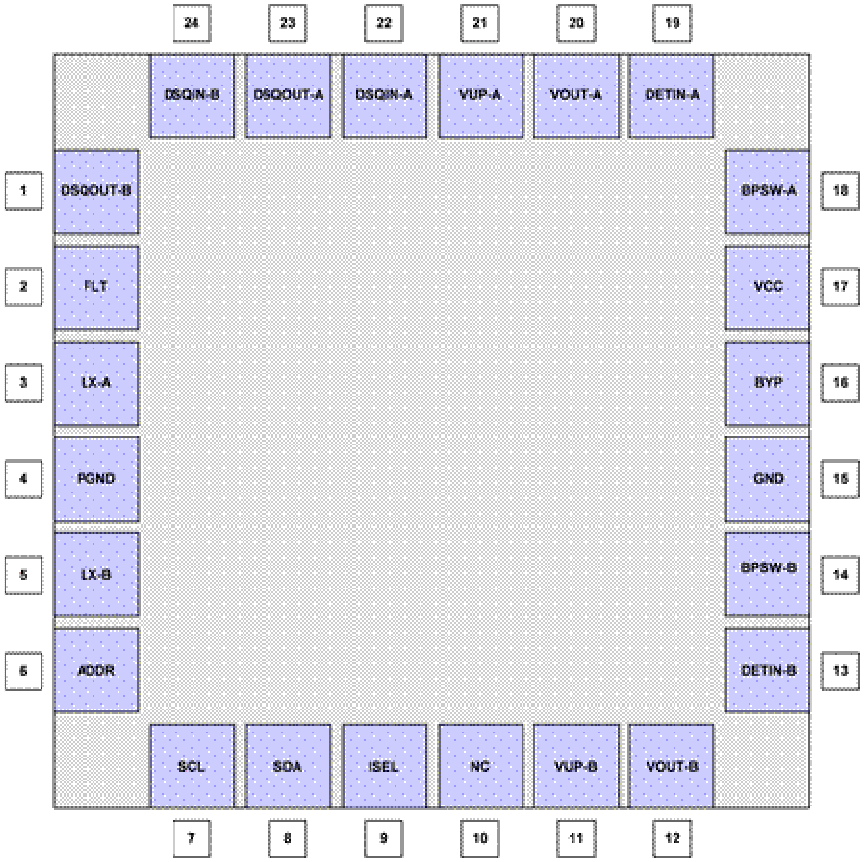
Lot #	Diffusion Lot	Assy Lot	Tech. Code	Process/ Package	Product Line	Comments
1	5226598	ENGC3402	AYD8*UI87AA5	BCD6S-3M/ HVQFN 4x4 24L	UI87	CUT1.0
2		ENGC4003				
3		ENGC3404	AY94*UI87AA5	BCD6S-3M/ MLPQHS 3x3 16L		

Test	PC	Std ref.	Conditions	Steps	Failure/SS			Note
					Lot 1	Lot 2	Lot 3	
Die Oriented Tests								
HTB	N	JESD22 A-108	Tj = 125°C, Vbias=+6V	168 H	0/77			
				500 H	0/77			
				1000 H	0/77			
HTSL	N	JESD22 A-103	Ta = 150°C	168 H	0/45	0/45	0/45	
				500 H	0/45	0/45	0/45	
				1000 H	0/45	0/45	0/45	
Package Oriented Tests								
PC		JESD22 A-113	Drying 24H@125°C Store 168H@Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times	Final	Pass	Pass	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	96 H	0/77	0/77	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	100 cy	0/77	0/77	0/77	
				200 cy	0/77	0/77	0/77	
				500 cy	0/77	0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85% Vbias=+5V,	168 H	0/77	0/77		
				500 H	0/77	0/77		
				1000 H	0/77	0/77		
Other Tests								
ESD	N	AEC Q101-001, 002 and 005	HBM	±2KV	Pass			All pins
				±8KV	Pass			I/O, RST, VCC, CLK,PRES Pins
			CDM	±500V	Pass	Pass	Pass	
			MM	±200V	Pass			
LU	N	AEC Q100 - 004	Current Inj. Overvoltage	±100mA	Pass			

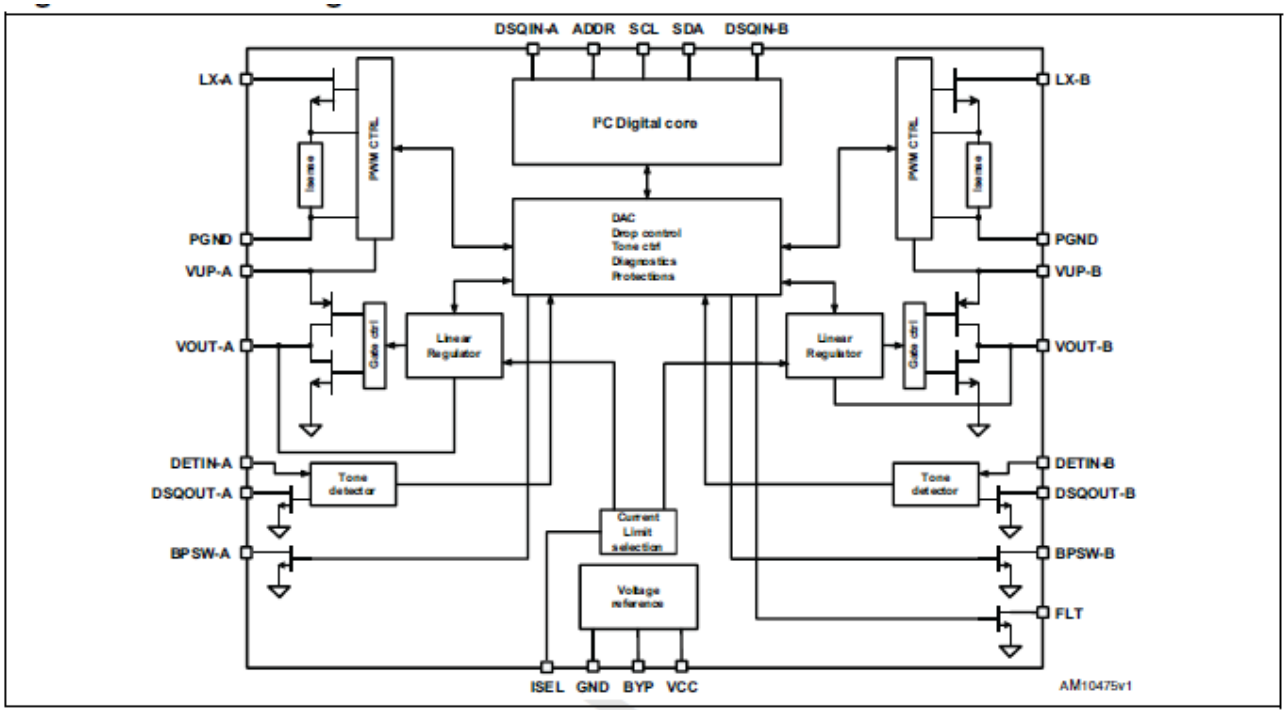
6 ANNEXES

6.1 Device details

6.1.1 Pin connection



6.1.2 Block diagram



6.2 Test Description

Test name	Description	Purpose
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HTB High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CBM: Charged Device Model HBM: Human Body Model MM: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

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