



FEMTOCLOCKS™ CRYSTAL-TO-LVDS FREQUENCY SYNTHESIZER W/INTEGRATED FANOUT BUFFER

ICS844256I

GENERAL DESCRIPTION



The ICS844256I is a Crystal-to-LVDS Clock Synthesizer/Fanout Buffer designed for SONET and Gigabit Ethernet applications and is a member of the HiperClockS™ family of High Performance Clock Solutions from IDT. The output frequency can be set using the frequency select pins and a 25MHz crystal for Ethernet frequencies, or a 19.44MHz crystal for SONET. The low phase noise characteristics of the ICS844256I make it an ideal clock for these demanding applications.

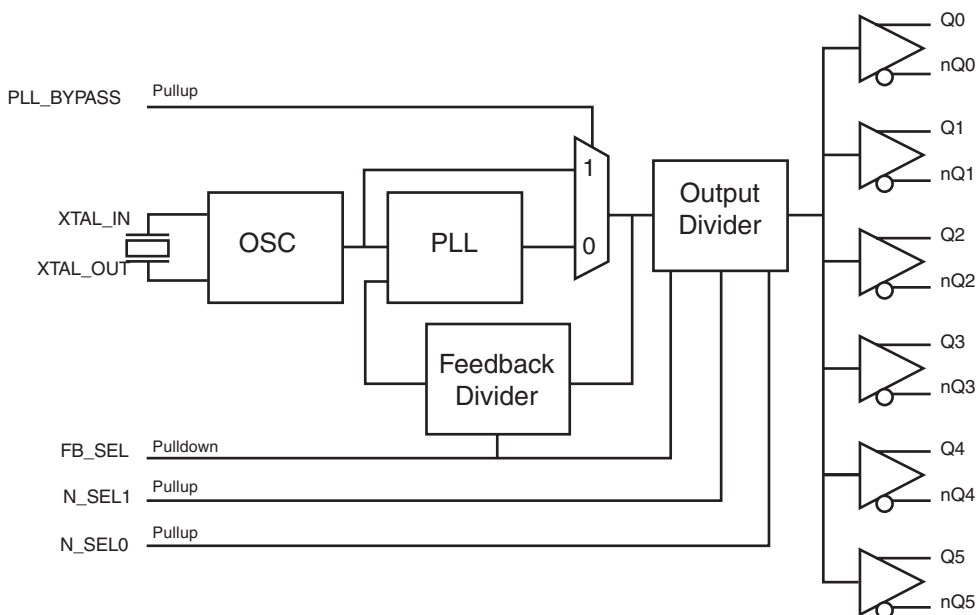
FEATURES

- Six LVDS outputs
- Crystal oscillator interface
- Output frequency range: 62.5MHz to 625MHz
- Crystal input frequency range: 15.625MHz to 25.5MHz
- RMS phase jitter at 125MHz, using a 25MHz crystal (1.875MHz to 20MHz): 0.48ps (typical)
- Full 3.3V or 3.3V core, 2.5V output supply mode
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

SELECT FUNCTION TABLE

| Inputs | | | Function | | |
|--------|--------|--------|----------|----------|------|
| FB_SEL | N_SEL1 | N_SEL0 | M Divide | N Divide | M/N |
| 0 | 0 | 0 | 25 | 1 | 25 |
| 0 | 0 | 1 | 25 | 2 | 12.5 |
| 0 | 1 | 0 | 25 | 4 | 6.25 |
| 0 | 1 | 1 | 25 | 5 | 5 |
| 1 | 0 | 0 | 32 | 1 | 32 |
| 1 | 0 | 1 | 32 | 2 | 16 |
| 1 | 1 | 0 | 32 | 4 | 8 |
| 1 | 1 | 1 | 32 | 8 | 4 |

BLOCK DIAGRAM



PIN ASSIGNMENT

| | | | |
|------------------|----|----|----------|
| V _{DD0} | 1 | 24 | Q3 |
| V _{DD0} | 2 | 23 | nQ3 |
| nQ2 | 3 | 22 | Q4 |
| Q2 | 4 | 21 | nQ4 |
| nQ1 | 5 | 20 | Q5 |
| Q1 | 6 | 19 | nQ5 |
| nQ0 | 7 | 18 | N_SEL1 |
| Q0 | 8 | 17 | GND |
| PLL_BYPASS | 9 | 16 | GND |
| V _{DDA} | 10 | 15 | N_SEL0 |
| V _{DD} | 11 | 14 | XTAL_OUT |
| FB_SEL | 12 | 13 | XTAL_IN |

ICS844256I
24-Lead TSSOP, E-Pad
 4.40mm x 7.8mm x 0.90mm
 body package
G Package
 Top View

TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|--------|-------------------|--------|----------|---|
| 1, 2 | V _{DDO} | Power | | Output supply pins. |
| 3, 4 | nQ2, Q2 | Output | | Differential output pair. LVDS interface levels. |
| 5, 6 | nQ1, Q1 | Output | | Differential output pair. LVDS interface levels. |
| 7, 8 | nQ0, Q0 | Output | | Differential output pair. LVDS interface levels. |
| 9 | PLL_BYPASS | Input | Pullup | Selects between the PLL and crystal inputs as the input to the dividers. When LOW, selects PLL. When HIGH, selects XTAL_IN, XTAL_OUT. LVCMOS / LVTTTL interface levels. |
| 10 | V _{DDA} | Power | | Analog supply pin. |
| 11 | V _{DD} | Power | | Core supply pin. |
| 12 | FB_SEL | Input | Pulldown | Feedback frequency select pin. LVCMOS/LVTTTL interface levels. |
| 13, 14 | XTAL_IN, XTAL_OUT | Input | | Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output. |
| 15, 18 | N_SEL0 N_SEL1 | Input | Pullup | Output frequency select pin. LVCMOS/LVTTTL interface levels. |
| 16, 17 | GND | | | Power supply ground. |
| 19, 20 | nQ5, Q5 | Output | | Differential output pair. LVDS interface levels. |
| 21, 22 | nQ4, Q4 | Output | | Differential output pair. LVDS interface levels. |
| 23, 24 | nQ3, Q3 | Output | | Differential output pair. LVDS interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |

CRYSTAL FUNCTION TABLE

| Inputs | | | | Function | | | |
|------------|--------|--------|--------|----------|-----------|---|--------------|
| XTAL (MHz) | FB_SEL | N_SEL1 | N_SEL0 | M | VCO (MHz) | N | Output (MHz) |
| 20 | 0 | 0 | 0 | 25 | 500 | 1 | 500 |
| 20 | 0 | 0 | 1 | 25 | 500 | 2 | 250 |
| 20 | 0 | 1 | 0 | 25 | 500 | 4 | 125 |
| 20 | 0 | 1 | 1 | 25 | 500 | 5 | 100 |
| 21.25 | 0 | 1 | 1 | 25 | 531.25 | 5 | 106.25 |
| 24 | 0 | 0 | 0 | 25 | 600 | 1 | 600 |
| 24 | 0 | 0 | 1 | 25 | 600 | 2 | 300 |
| 24 | 0 | 1 | 0 | 25 | 600 | 4 | 150 |
| 24 | 0 | 1 | 1 | 25 | 600 | 5 | 120 |
| 25 | 0 | 0 | 0 | 25 | 625 | 1 | 625 |
| 25 | 0 | 0 | 1 | 25 | 625 | 2 | 312.5 |
| 25 | 0 | 1 | 0 | 25 | 625 | 4 | 156.25 |
| 25 | 0 | 1 | 1 | 25 | 625 | 5 | 125 |
| 25.5 | 0 | 1 | 0 | 25 | 637.5 | 4 | 159.375 |
| 15.625 | 1 | 1 | 1 | 32 | 500 | 8 | 62.5 |
| 18.5625 | 1 | 1 | 1 | 32 | 594 | 8 | 74.25 |
| 18.75 | 1 | 0 | 0 | 32 | 600 | 1 | 600 |
| 18.75 | 1 | 0 | 1 | 32 | 600 | 2 | 300 |
| 18.75 | 1 | 1 | 0 | 32 | 600 | 4 | 150 |
| 18.75 | 1 | 1 | 1 | 32 | 600 | 8 | 75 |
| 19.44 | 1 | 0 | 0 | 32 | 622.08 | 1 | 622.08 |
| 19.44 | 1 | 0 | 1 | 32 | 622.08 | 2 | 311.04 |
| 19.44 | 1 | 1 | 0 | 32 | 622.08 | 4 | 155.52 |
| 19.44 | 1 | 1 | 1 | 32 | 622.08 | 8 | 77.76 |
| 19.53125 | 1 | 0 | 0 | 32 | 625 | 1 | 625 |
| 19.53125 | 1 | 0 | 1 | 32 | 625 | 2 | 312.5 |
| 19.53125 | 1 | 1 | 0 | 32 | 625 | 4 | 156.25 |
| 19.53125 | 1 | 1 | 1 | 32 | 625 | 8 | 78.125 |
| 20 | 1 | 1 | 1 | 32 | 640 | 8 | 80 |

ABSOLUTE MAXIMUM RATINGS

| | |
|--|--------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, I_O | |
| Continuous Current | 10mA |
| Surge Current | 15mA |
| Package Thermal Impedance, θ_{JA} | |
| 24 Lead TSSOP, EPad | 32.1°C/W (0 mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|-----------------|---------|----------|-------|
| V_{DD} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDA} | Analog Supply Voltage | | $V_{DD} - 0.20$ | 3.3 | V_{DD} | V |
| V_{DDO} | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{DD} | Power Supply Current | | | | 160 | mA |
| I_{DDA} | Analog Supply Current | | | | 20 | mA |
| I_{DDO} | Output Supply Current | | | | 160 | mA |

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|-----------------|---------|----------|-------|
| V_{DD} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDA} | Analog Supply Voltage | | $V_{DD} - 0.20$ | 3.3 | V_{DD} | V |
| V_{DDO} | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| I_{DD} | Power Supply Current | | | | 160 | mA |
| I_{DDA} | Analog Supply Current | | | | 20 | mA |
| I_{DDO} | Output Supply Current | | | | 150 | mA |

TABLE 4C. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|-------------------------------|--------------------------------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | FB_SEL | $V_{DD} = V_{IN} = 3.465V$ | | 150 | μA |
| | | PLL_BYPASS, N_SEL0, N_SEL1 | $V_{DD} = V_{IN} = 3.465V$ | | 5 | μA |
| I_{IL} | Input Low Current | FB_SEL | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5 | | μA |
| | | PLL_BYPASS, N_SEL0, N_SEL1 | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150 | | μA |

TABLE 4D. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ $T_A = -40^\circ\text{C}$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| V_{OD} | Differential Output Voltage | | | 350 | | mV |
| ΔV_{OD} | V_{OD} Magnitude Change | | | 40 | | mV |
| V_{OS} | Offset Voltage | | | 1.25 | | V |
| ΔV_{OS} | V_{OS} Magnitude Change | | | 50 | | mV |

NOTE: Please refer to Parameter Measurement Information for output information.

TABLE 4E. LVDS DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| V_{OD} | Differential Output Voltage | | | 350 | | mV |
| ΔV_{OD} | V_{OD} Magnitude Change | | | 40 | | mV |
| V_{OS} | Offset Voltage | | | 1.25 | | V |
| ΔV_{OS} | V_{OS} Magnitude Change | | | 50 | | mV |

TABLE 5. CRYSTAL CHARACTERISTICS

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 15.625 | | 25.5 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |
| Drive Level | | | | 1 | mW |

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|---------------------------|--|---------|---------|---------|-------|
| F_{OUT} | Output Frequency | | 53.125 | | 333.33 | MHz |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter (Random) | 125MHz, Integration Range: 1.875MHz - 20MHz | | 0.33 | | ps |
| $t_{sk}(o)$ | Output Skew; NOTE 1, 2 | | | 65 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 200 | | 550 | ps |
| odc | Output Duty Cycle | $\leq 312.5MHz$ | 47 | | 53 | % |
| | | $> 312.5MHz$ | 42 | | 58 | % |
| t_{LOCK} | PLL Lock Time | | | | 1 | ms |

See Parameter Measurement Information section.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential crossing points.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6B. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|---------------------------|--|---------|---------|---------|-------|
| F_{OUT} | Output Frequency | | 53.125 | | 333.33 | MHz |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter (Random) | 125MHz, Integration Range: 1.875MHz - 20MHz | | 0.32 | | ps |
| $t_{sk}(o)$ | Output Skew; NOTE 1, 2 | | | 60 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 140 | | 600 | ps |
| odc | Output Duty Cycle | $\leq 312.5MHz$ | 46 | | 54 | % |
| | | $> 312.5MHz$ | 40 | | 60 | % |
| t_{LOCK} | PLL Lock Time | | | | 1 | ms |

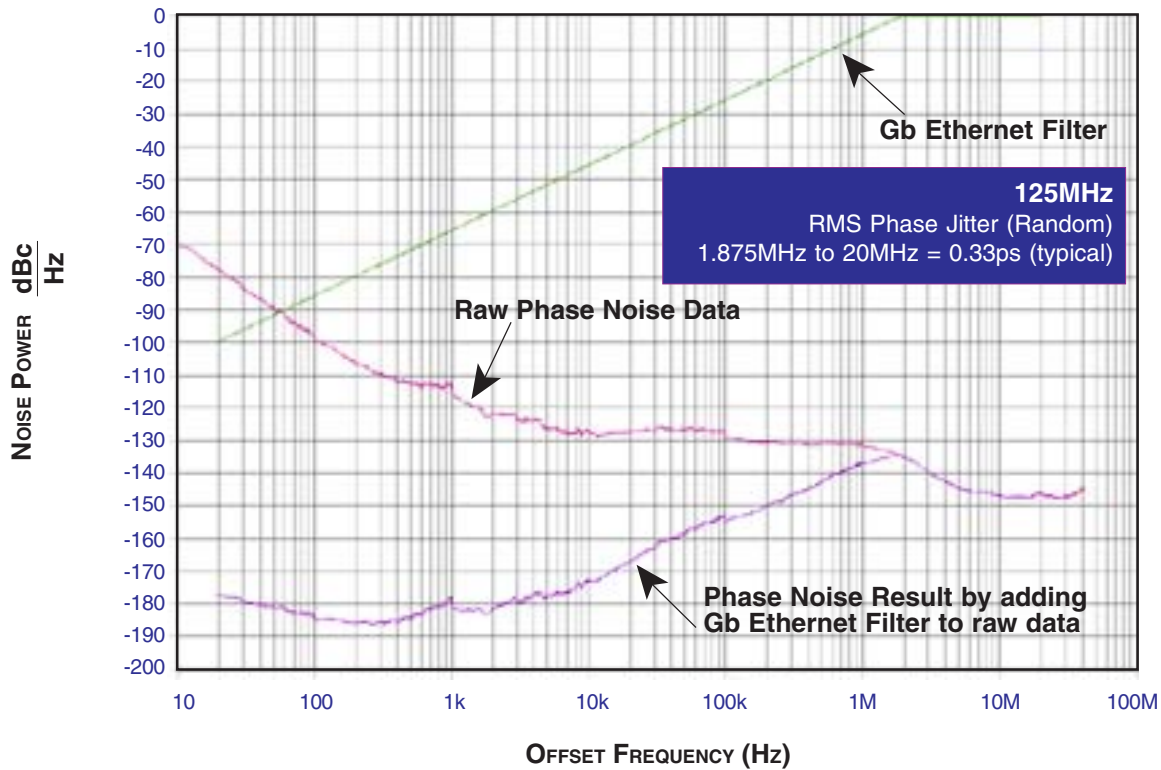
See Parameter Measurement Information section.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions.

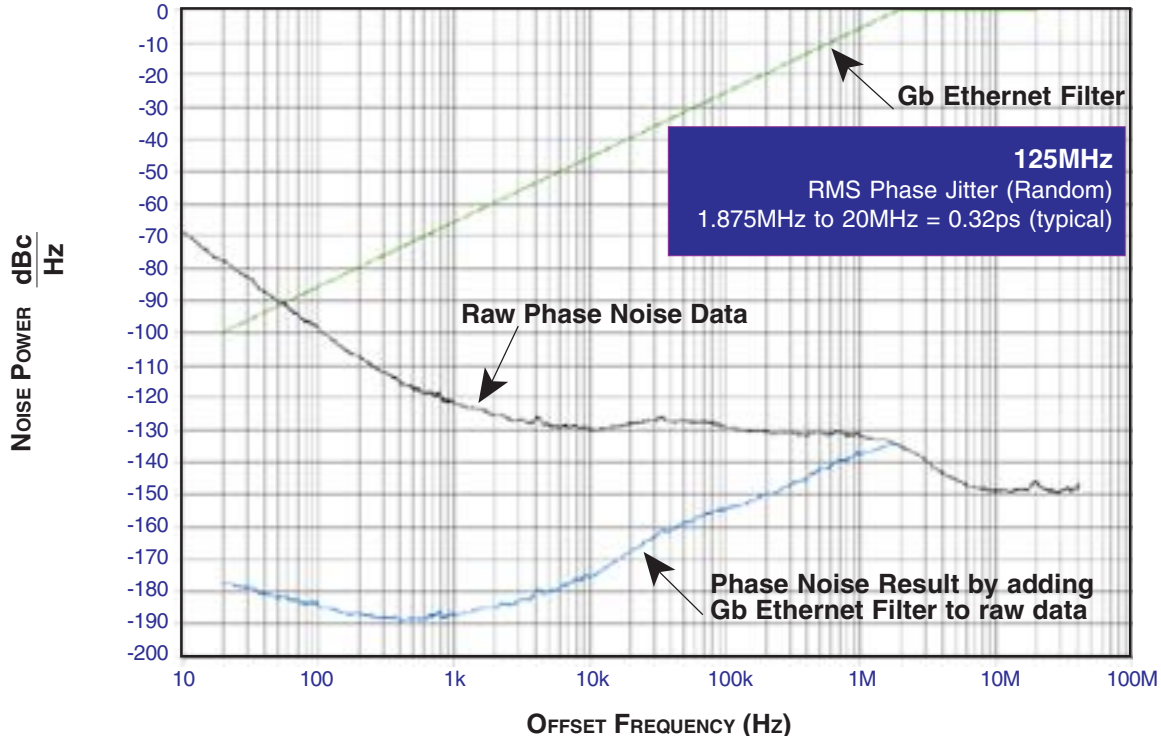
Measured at the output differential crossing points.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

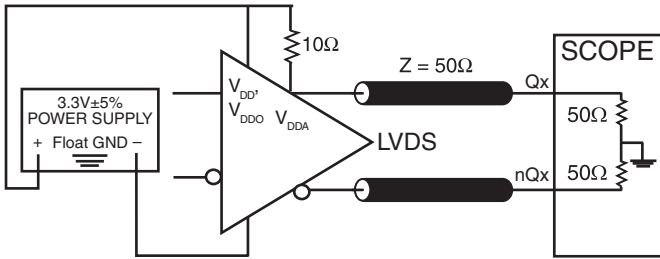
TYPICAL PHASE NOISE AT 125MHz @ 3.3V



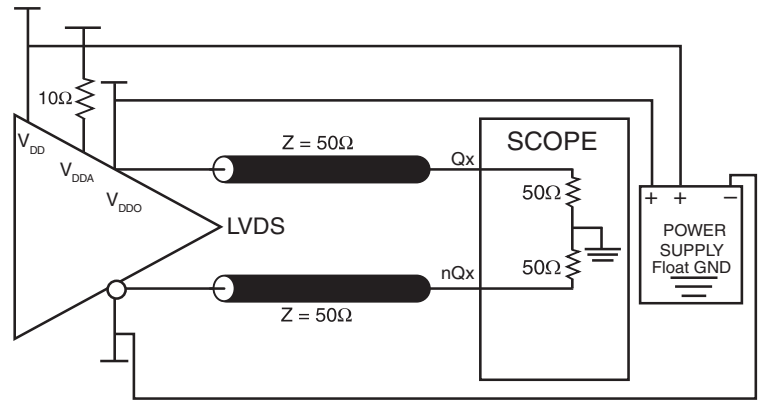
TYPICAL PHASE NOISE AT 125MHz @ 3.3V/2.5V



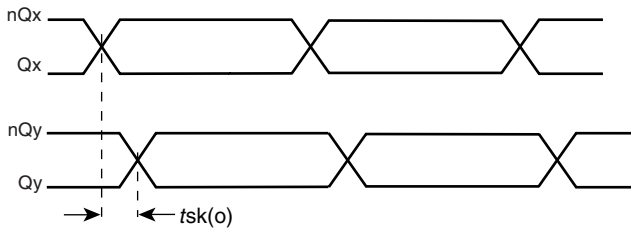
PARAMETER MEASUREMENT INFORMATION



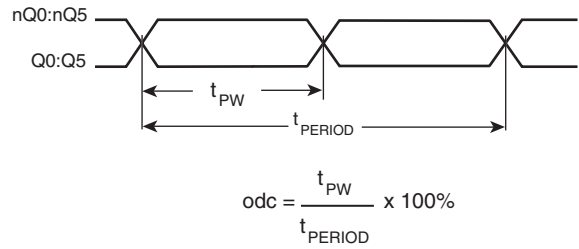
3.3V OUTPUT LOAD AC TEST CIRCUIT



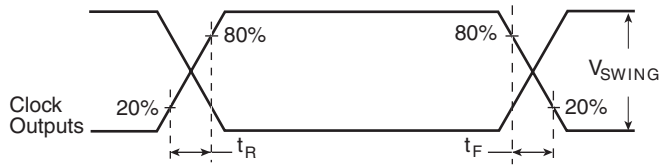
3.3V/2.5V OUTPUT LOAD AC TEST CIRCUIT



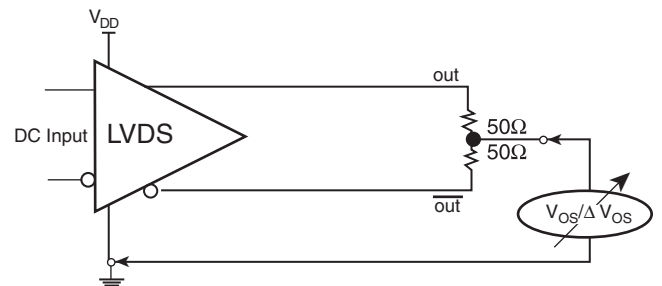
OUTPUT SKEW



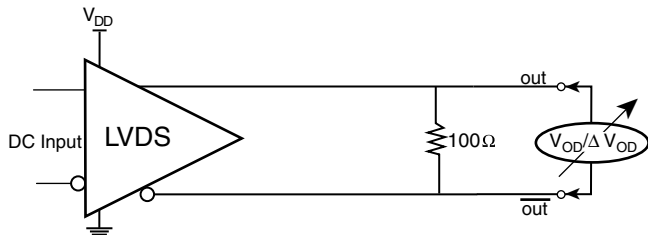
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS844256I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} , and V_{DDO} should be individually connected to the power supply plane through vias, and $0.01\mu\text{F}$ bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a $10\mu\text{F}$ bypass capacitor be connected to the V_{DDA} pin.

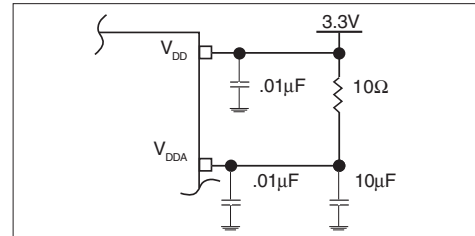


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVC MOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A $1\text{k}\Omega$ resistor can be used.

OUTPUTS:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

CRYSTAL INPUT INTERFACE

The ICS844256I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2*

below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

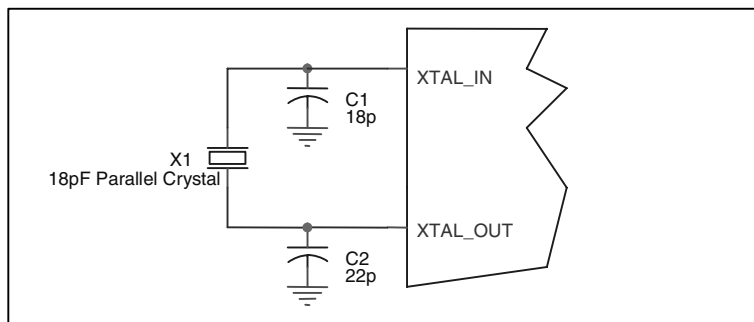


FIGURE 2. CRYSTAL INPUT INTERFACE

LVC MOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVC MOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 3*. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (R_o) plus the series

resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50Ω applications, R_1 and R_2 can be 100Ω. This can also be accomplished by removing R_1 and making R_2 50Ω.

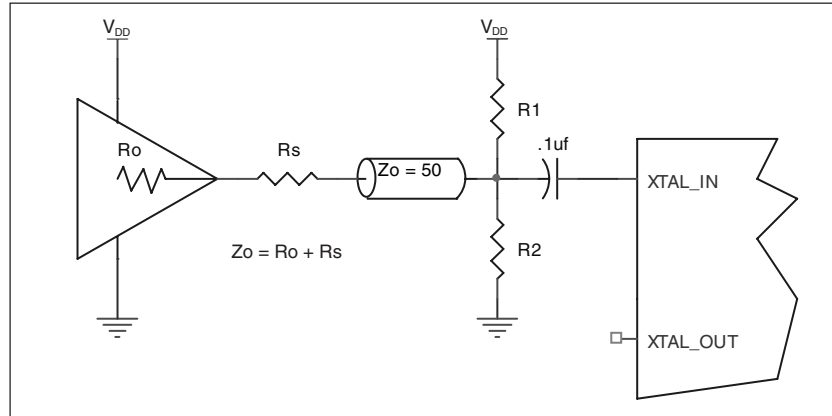


FIGURE 3. GENERAL DIAGRAM FOR LVC MOS DRIVER TO XTAL INPUT INTERFACE

3.3V, 2.5V LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 4*. In a 100Ω differential transmission line environment, LVDS drivers

require a matched load termination of 100Ω across near the receiver input.

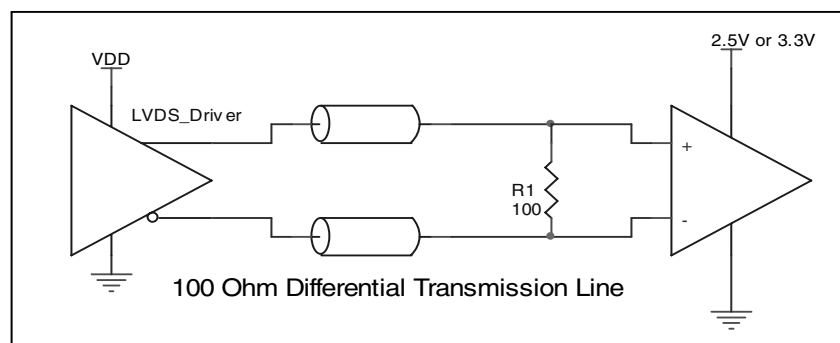


FIGURE 4. TYPICAL LVDS DRIVER TERMINATION

EPAD THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”)

are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

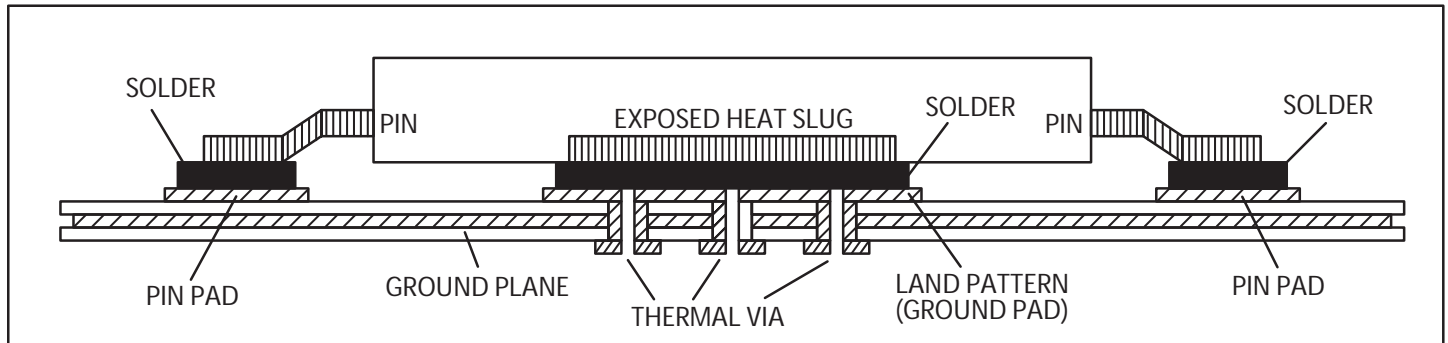


FIGURE 5. ASSEMBLY FOR EXPOSED PAD THERMAL RELEASE PATH –SIDE VIEW (DRAWING NOT TO SCALE)

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS844256I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844256I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

- Power (core)_{MAX} = $V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (160mA + 20mA) = 623.7mW$
- Power (outputs)_{MAX} = $V_{DDO_MAX} * I_{DDO_MAX} = 3.465V * 160mA = 554.4mW$

$$\text{Total Power}_{_MAX} = 623.7mW + 554.4mW = 1178mW$$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 32.1°C/W per Table 7 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 1.178\text{W} * 32.1^\circ\text{C/W} = 122.8^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 24-LEAD TSSOP, E-PAD, FORCED CONVECTION

| θ_{JA} by Velocity (Meters per Second) | | | |
|---|----------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 32.1°C/W | 25.5°C/W | 24.0°C/W |

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP, E-PAD

| θ_{JA} by Velocity (Meters per Second) | | | |
|---|----------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 32.1°C/W | 25.5°C/W | 24.0°C/W |

TRANSISTOR COUNT

The transistor count for ICS844256I is: 3887

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP, E-PAD

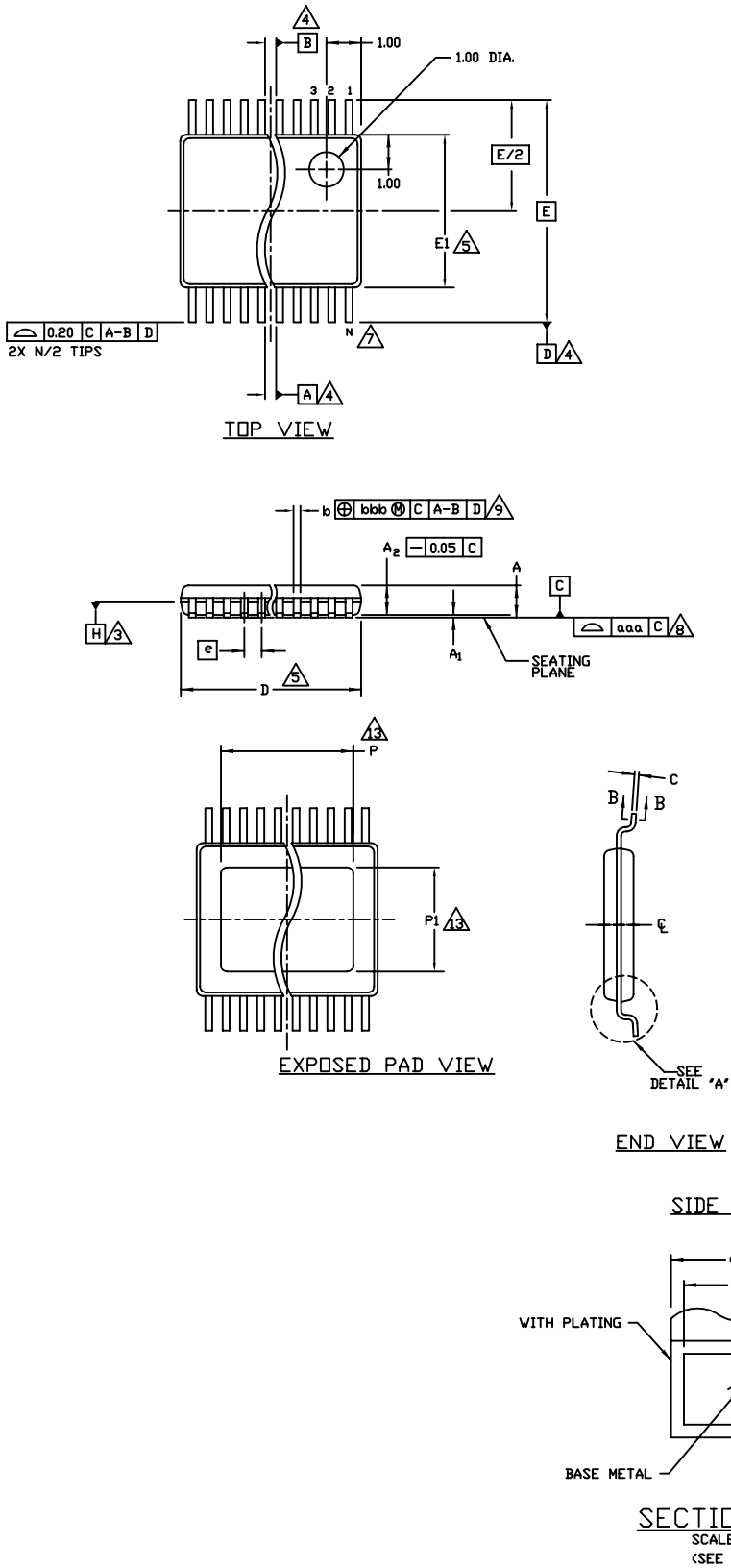


TABLE 9. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | | |
|----------|-------------|---------|---------|
| | Minimum | Nominal | Maximum |
| N | 24 | | |
| A | -- | | 1.10 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.85 | 0.90 | 0.95 |
| b | 0.19 | | 0.30 |
| b1 | 0.19 | 0.22 | 0.25 |
| c | 0.09 | | 0.20 |
| c1 | 0.09 | 0.127 | 0.16 |
| D | 7.70 | 7.80 | 7.90 |
| E | 6.40 BASIC | | |
| E1 | 4.30 | 4.40 | 4.50 |
| e | 0.65 BASIC | | |
| L | 0.50 | 0.60 | 0.70 |
| P | | | 5.0 |
| P1 | | | 3.2 |
| α | 0° | | 8° |
| aaa | 0.076 | | |
| bbb | 0.10 | | |

Reference Document: JEDEC Publication 95, MO-153

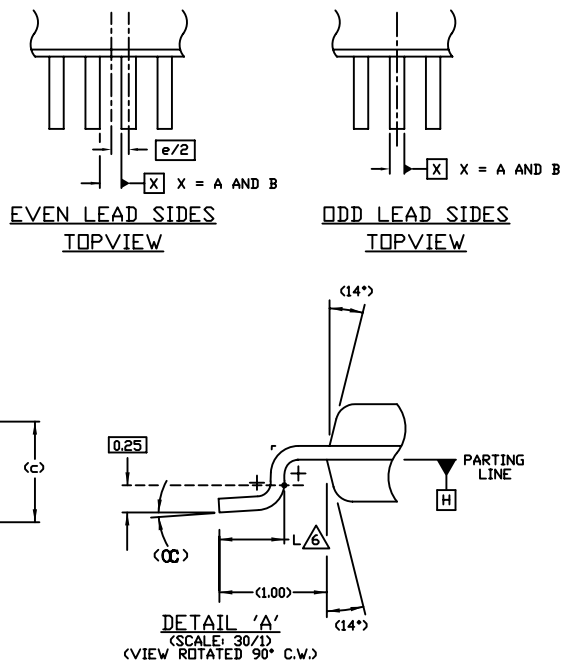


TABLE 10. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|---------------|----------------------------------|--------------------|---------------|
| ICS844256BGI | ICS844256BGI | 24 Lead TSSOP, E-Pad | tube | -40°C to 85°C |
| ICS844256BGIT | ICS844256BGI | 24 Lead TSSOP, E-Pad | 2500 tape & reel | -40°C to 85°C |
| ICS844256BGILF | ICS844256BGIL | 24 Lead "Lead-Free" TSSOP, E-Pad | tube | -40°C to 85°C |
| ICS844256BGILFT | ICS844256BGIL | 24 Lead "Lead-Free" TSSOP, E-Pad | 2500 tape & reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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