Ordering number : ENA0746C

SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

N-Channel Silicon MOSFET

2SK4124 — General-Purpose Switching Device Applications

Features

- Low ON-resistance, low input capacitance, ultrahigh-speed switching
- Adoption of high reliability HVP process
- Avalanche resistance guarantee

Specifications

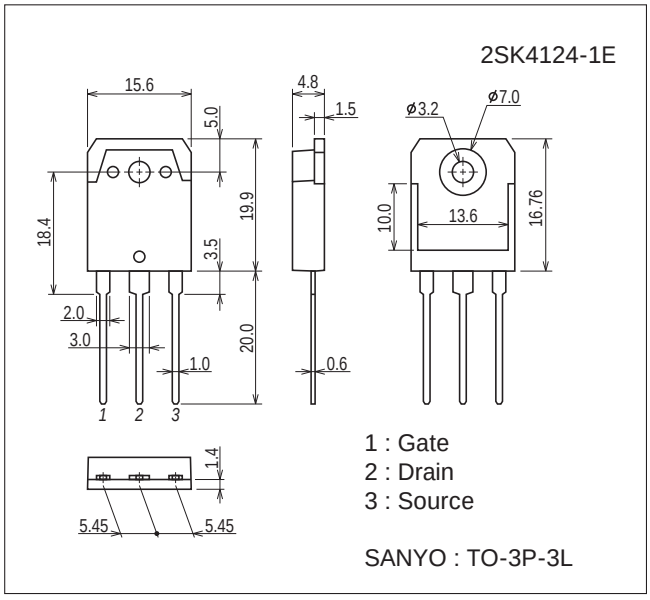
Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		500	V
Gate-to-Source Voltage	V_{GSS}		±30	V
Drain Current (DC)	I_D		20	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	60	A
Allowable Power Dissipation	P_D		2.5	W
		Tc=25°C (SANYO's ideal heat dissipation condition)*1	170	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		−55 to +150	°C
Avalanche Energy (Single Pulse) *1	E_{AS}		110	mJ
Avalanche Current *2	I_{AV}		20	A

*1 SANYO's condition is radiation from backside.
The method is applying silicone grease to the backside of the device and attaching the device to water-cooled radiator made of aluminium.
*2 V_{DD}=50V, L=500μH, I_{AV}=20A (Fig.1)
*3 L≤500μH, single pulse

Package Dimensions

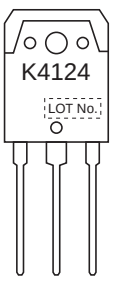
unit : mm (typ)
7539-002



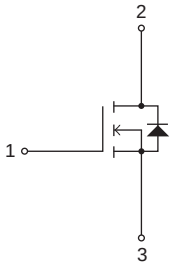
Product & Package Information

- Package : TO-3P-3L
- JEITA, JEDEC : SC-65, TO-247, SOT-199
- Minimum Packing Quantity : 30 pcs./magazine

Marking



Electrical Connection



Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0V	500			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=400V, V_{GS}=0V			100	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V			±100	nA
Cutoff Voltage	V_{GS}(off)	V_{DS}=10V, I_D=1mA	3		5	V
Forward Transfer Admittance	| yfs |	V_{DS}=10V, I_D=10A	4.9	9.7		S
Static Drain-to-Source On-State Resistance	R_{DS}(on)	I_D=8A, V_{GS}=10V		0.33	0.43	Ω
Input Capacitance	Ciss	V_{DS}=30V, f=1MHz		1200		pF
Output Capacitance	Coss			250		pF
Reverse Transfer Capacitance	Crss			55		pF
Turn-ON Delay Time	t_d(on)	See Fig.2		26.5		ns
Rise Time	t_r			95		ns
Turn-OFF Delay Time	t_d(off)			145		ns
Fall Time	t_f			58		ns
Total Gate Charge	Qg	V_{DS}=200V, V_{GS}=10V, I_D=20A		46.6		nC
Gate-to-Source Charge	Qgs			8.7		nC
Gate-to-Drain “Miller” Charge	Qgd			27.3		nC
Diode Forward Voltage	V_{SD}	I_S=20A, V_{GS}=0V		1.0	1.3	V

Fig.1 Avalanche Resistance Test Circuit

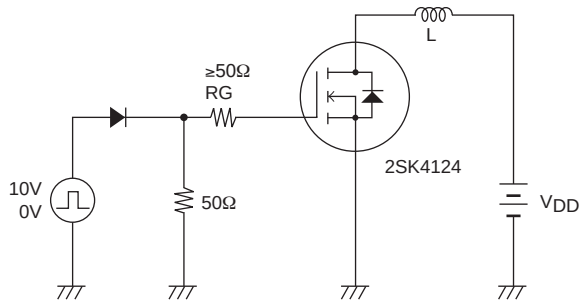
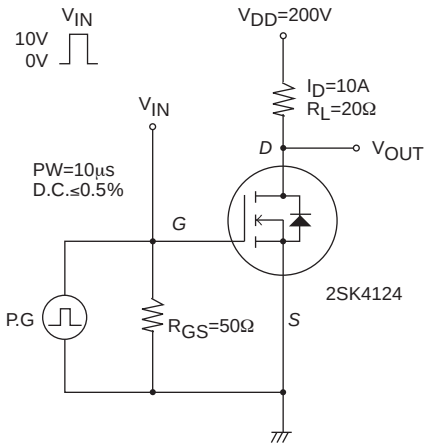
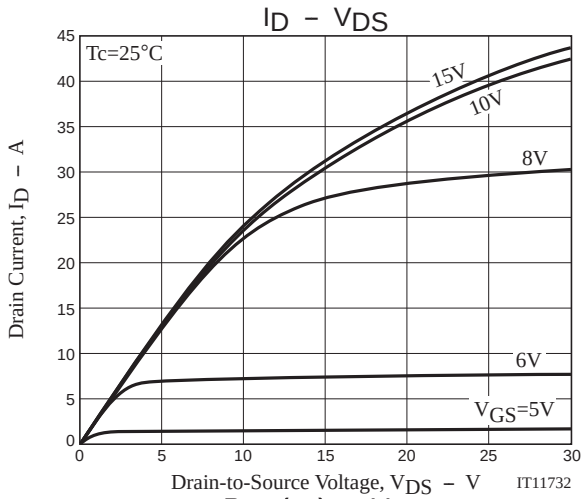


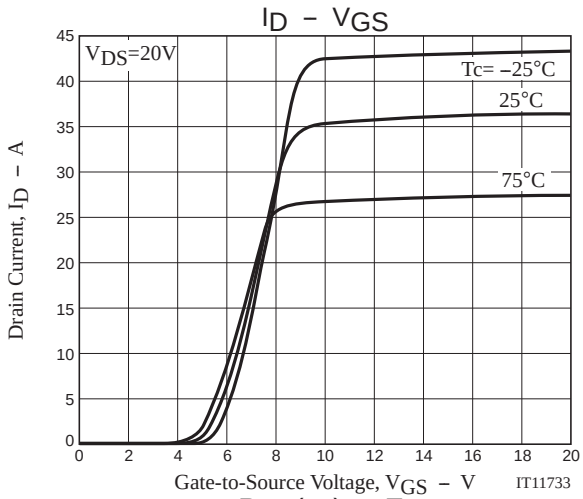
Fig.2 Switching Time Test Circuit

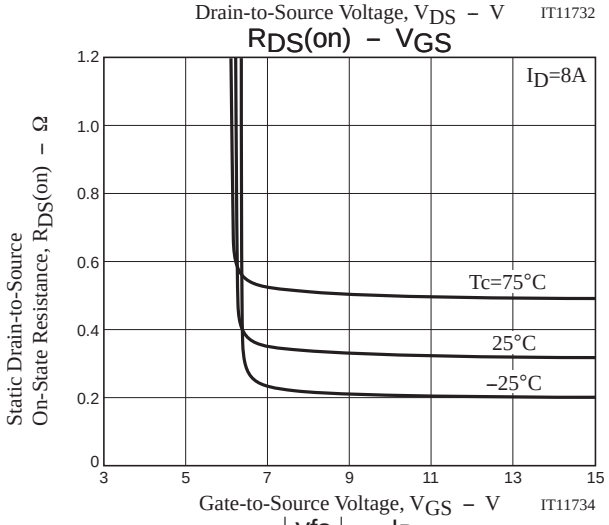


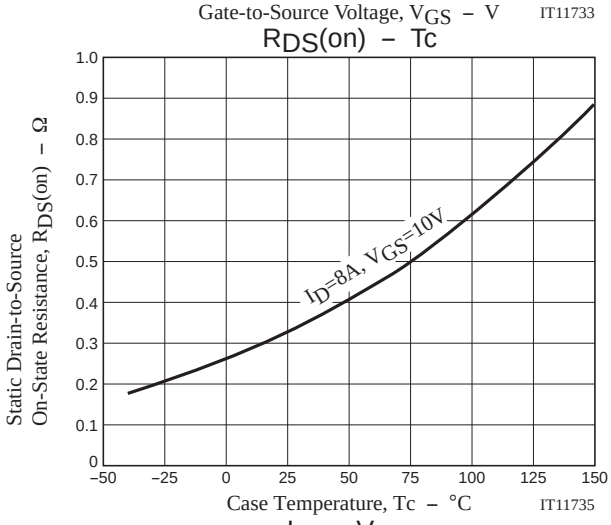
Ordering Information

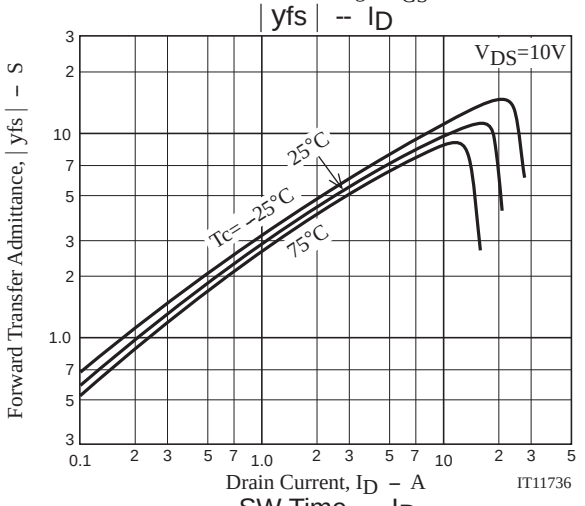
Device	Package	Shipping	memo
2SK4124-1E	TO-3P-3L	30pcs./magazine	Pb Free

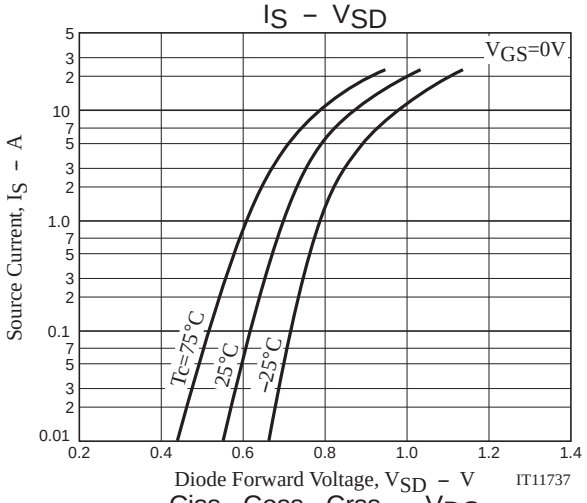

ID – VDS
Tc=25°C
15V
10V
8V
6V
VGS=5V
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT11732

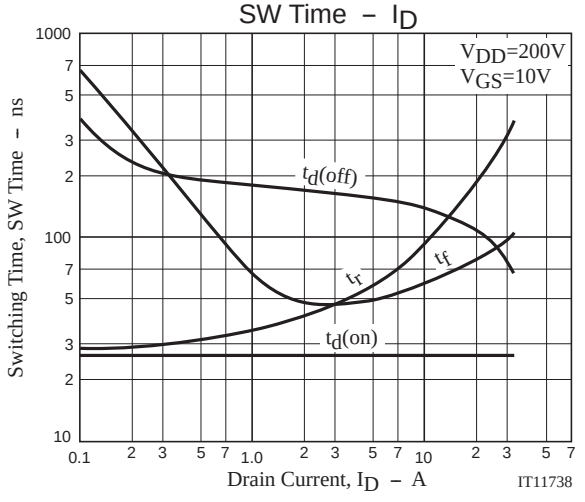

ID – VGS
VDS=20V
Tc= –25°C
25°C
75°C
Drain Current, ID – A
Gate-to-Source Voltage, VGS – V
IT11733

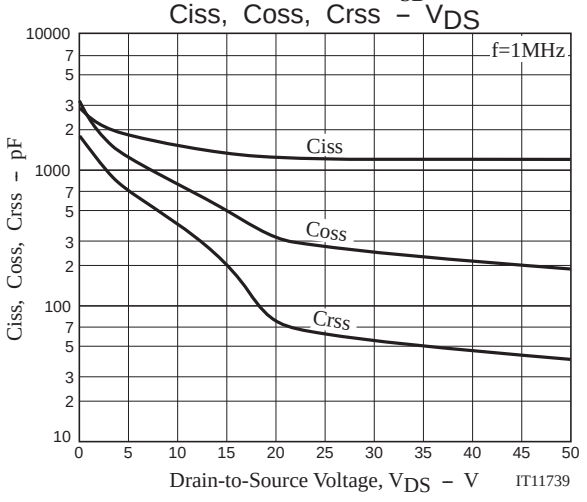

RDS(on) – VGS
ID=8A
Tc=75°C
25°C
–25°C
Static Drain-to-Source On-State Resistance, RDS(on) – Ω
Gate-to-Source Voltage, VGS – V
IT11734

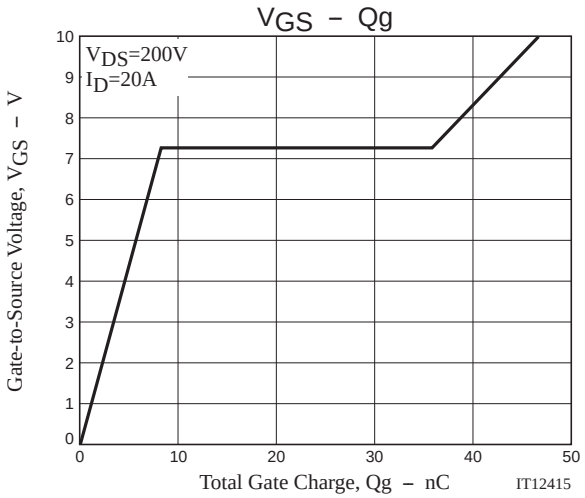

RDS(on) – Tc
ID=8A, VGS=10V
Static Drain-to-Source On-State Resistance, RDS(on) – Ω
Case Temperature, Tc – °C
IT11735

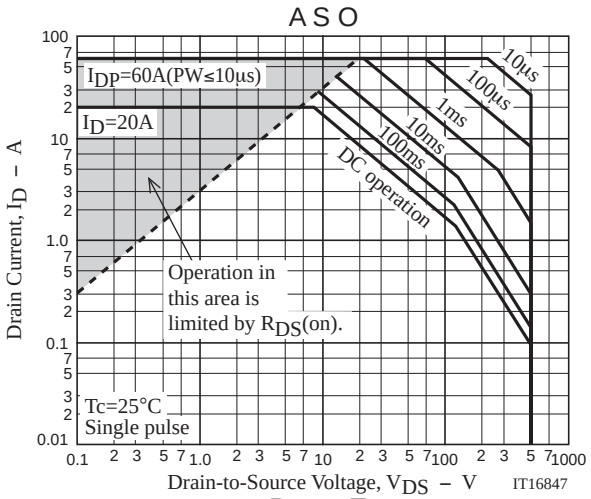

| yfs | -- ID
VDS=10V
25°C
Tc= –25°C
75°C
Forward Transfer Admittance, | yfs | – S
Drain Current, ID – A
IT11736

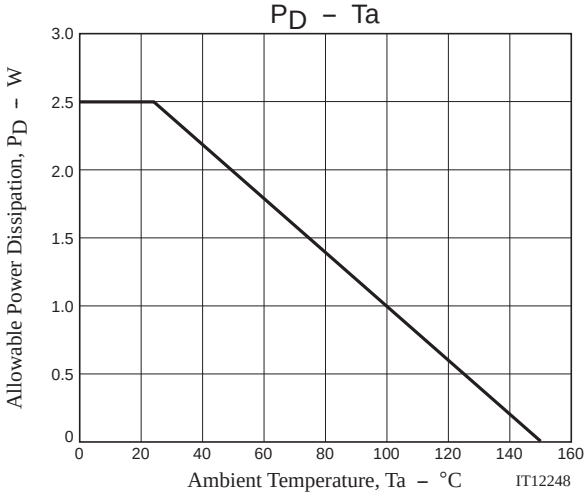

IS – VSD
VGS=0V
Tc=75°C
25°C
–25°C
Source Current, IS – A
Diode Forward Voltage, VSD – V
IT11737

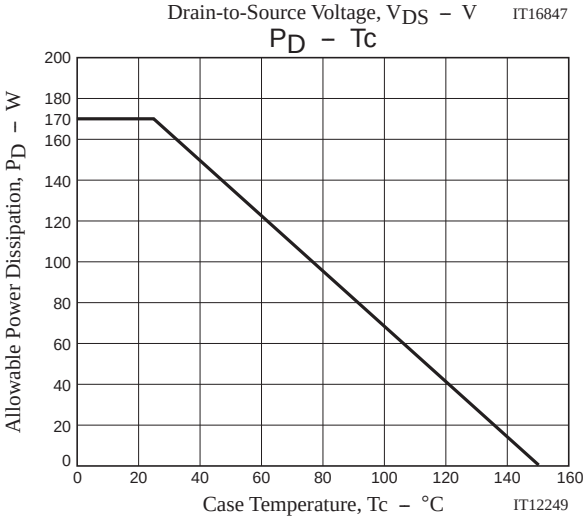

SW Time – ID
VDD=200V
VGS=10V
td(off)
tf
tr
td(on)
Switching Time, SW Time – ns
Drain Current, ID – A
IT11738

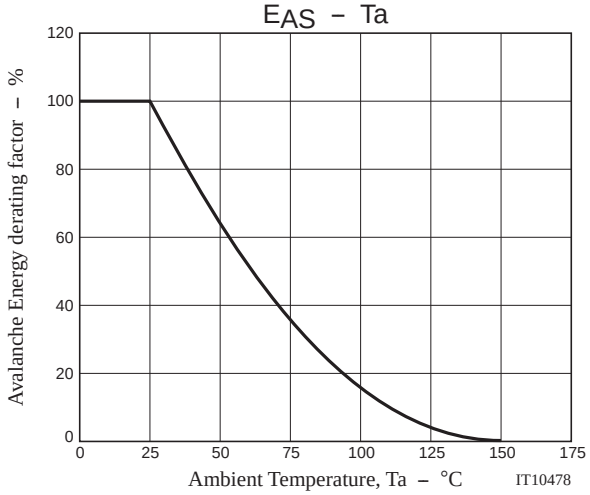

Ciss, Coss, Crss – VDS
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, VDS – V
IT11739


VGS – Qg
VDS=200V
ID=20A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT12415


A S O
IDP=60A(PW≤10μs)
ID=20A
10μs
100μs
1ms
10ms
100ms
DC operation
Operation in this area is limited by RDS(on).
Tc=25°C
Single pulse
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT16847


PD – Ta
Allowable Power Dissipation, PD – W
Ambient Temperature, Ta – °C
IT12248


PD – Tc
Allowable Power Dissipation, PD – W
Case Temperature, Tc – °C
IT12249


EAS – Ta
Avalanche Energy derating factor – %
Ambient Temperature, Ta – °C
IT10478

Magazine Specification

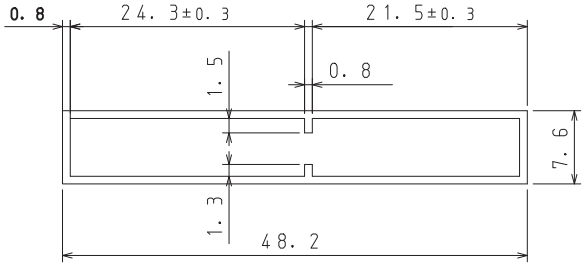
2SK4124-1E

1. Packing Format

Package Name	Maximum Number of devices contained (pcs)			Packing format	
	Magazine	Inner box	Outer box	Inner BOX	Outer BOX
TO-3P-3L	30	450	1800	SPD-0V0001 15 magazines contained Dimensions:mm(external) 568×150×55	SPD-LV0010 4 inner boxes contained Dimensions:mm(external) 590x225x178

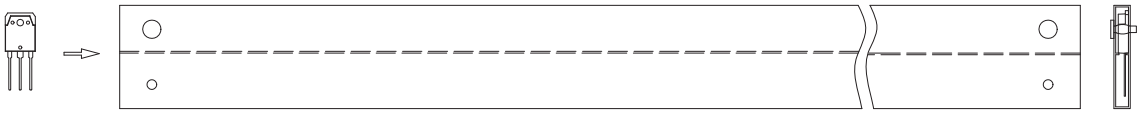
2. Magazine dimensions

(unit:mm)

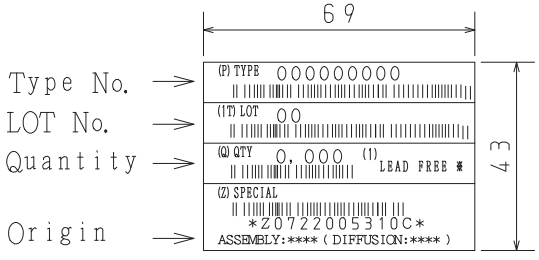


Tolerance=±0.2mm
Thickness=0.8±0.2mm
Length =508.0±1mm
Material =PVC or PET
(Antistatic treatment)

3. Storage method to magazine

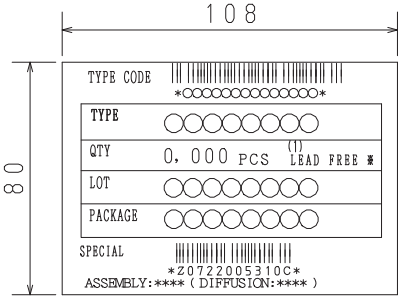


4. Inner box label (unit:mm)



5. Outer box label (unit:mm)

It is a label at the time of factory shipments.
The form of a label may change in physical distribution process.

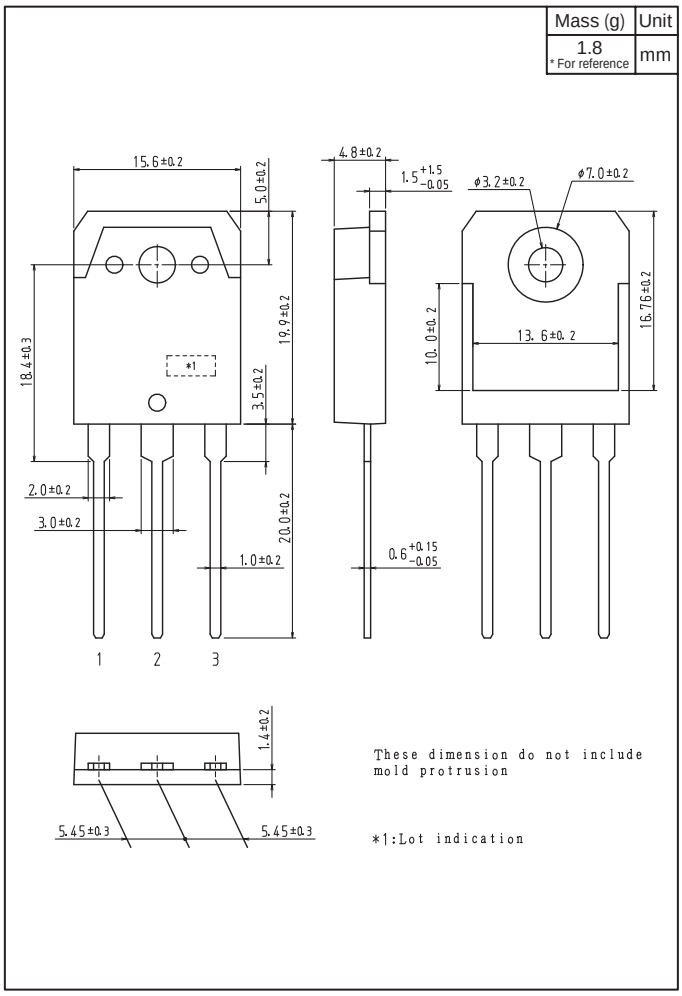


NOTE (1)
The LEAD FREE ※ description shows that the surface treatment of the terminal is lead free.

Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A

Outline Drawing

2SK4124-1E



Note on usage : Since the 2SK4124 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

This catalog provides information as of May, 2012. Specifications and information herein are subject to change without notice.